ADTRAN, INC, Plaintiff, v. TQ DELTA, LLC, Defendant	)	C.A. No. 1: 15-cv-121-RGA

DECLARATION OF DR. TODOR COOKLEV IN SUPPORT OF TQ DELTA'S FAMILY 3 CLAIM CONSTRUCTION BRIEF

I. Introduction

1. My name is Todor Cooklev, and I have been retained by complainant TQ Delta LLC (collectively, "TQ Delta").

2. I have been asked to prepare this Declaration in connection with the above captioned District Court actions, and have been asked to investigate and opine on issues relating to certain claim limitations of U.S. Patent Nos. 7,831,890 ("the '890 patent"), 7,836,381 ("the '381 patent"), 7,844,882 ("the '882 patent"), 8,276,048 ("the '048 patent"), 8,495,473 ("the '873 patent") and 8,607,126 ("the '126 patent"), hereinafter the "Family 3 Patents," that TQ Delta believes need construction.

3. I previously prepared a declaration in these actions, the Declaration of Dr. Todor Cooklev in Support of TQ Delta's Family 2 Claim Construction Brief, dated June 14, 2017. My previous declaration included a summary of my qualifications as well as a list of materials considered in forming my opinions in this matter, which I incorporate by reference. (*See* Cooklev June 14, 2017 Decl. at ¶¶ 7-14.)

4. I based this Declaration on information currently available to me. I reserve the right to continue my investigation. I further reserve the right to expand, modify, and/or supplement this Declaration and my opinions as additional information becomes available to me, including in response to matters raised by the defendants and/or defendants' expert(s), or in view of relevant orders and findings by the Court.

5. In this Report, I cite to various documents and testimony. These citations are meant to be exemplary, and not exhaustive. Citations to documents or testimony are not intended to signify that my conclusions or opinions are limited to the cited sources, or supported by the cited sources only.

6. In particular, this declaration addresses the following claim terms:

Term	Claims
transceiver	'890 patent, claim 5, '381 patent, claim 5 '882 patent, claim 13, '048 patent, claim 1, '473 patent, claim 19, 28, and '126 patent, claims 1, 10
"shared memory"	'890 patent, claim 5, '381 patent, claim 5, '882 patent, claim 13, and '048 patent, claim 1
"the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]"	'890 patent, claim 5, '381 patent, claim 5, '882 patent, claim 13, and '048 patent, claim 1

II. Materials Considered

7. In forming my opinions expressed in this declaration, I have considered and relied upon my education, background, and experience. In addition to the materials listed in my previous declaration, I have also reviewed the Family 3 patents and their file histories:

- U.S. 7,831,890 to Tzannes, an Asserted Patent in Family 3, A1-12;
- U.S. 7,836,381 to Tzannes, an Asserted Patent in Family 3, A13-24
- U.S. 7,844,882 to Tzannes, an Asserted Patent in Family 3, A25-A36;
- U.S. 8,276,048 to Tzannes, an Asserted Patent in Family 2, A37-A49;
- U.S. 8,495,473 to Tzannes, an Asserted Patent in Family 2, A50-A62;
- U.S. 8,607,126 to Tzannes, an Asserted Patent in Family 3, A63-74.

III. Applicable Legal Standards

8. I understand that a patent specification is required to conclude with one or more claims that particularly point out and distinctly claim the subject matter that the patent applicant regards as his invention. This requires that a patent's claims, viewed in light of the specification and prosecution history, inform a person of ordinary skill in the art about the scope of the invention with reasonable certainty.

IV. Level of Ordinary Skill in the Art

9. A person of ordinary skill in the art at or before the time of the inventions of the Family 3 patents would have had a bachelor's degree in electrical engineering with 2-3 years of experience in DSL communication systems. Alternatively, the person would have had a master's degree in electrical engineering. I am familiar with the knowledge and capabilities of one or ordinary skill in this area based on my experience working with industry, with undergraduate and graduate students, with colleagues from academia, and with engineers practicing in the industry.

V. Background of the Technology

10. The following section provides an overview of the field of the inventions and the specific subject matter claimed in the Family 3 patents. To facilitate an understanding of the inventions also included is a description of the state of art and concepts important to understand the claimed inventions.

11. Data communication between two communication endpoints, a first (near end) and second (far end) transceiver for example, is effected by communicating one or more bits of data (data bits) serially. The data bits are communicated over a communication medium that may be, for example, a phone line. In one exemplary scheme, bits of data are communicated serially in the form of a bit stream. In another exemplary scheme, DMT for example, groups of bits of data are communicated serially. An illustration of a bit stream is shown below. Each white box represents a single bit or a group of data bits.

12. The Family 3 patents relate to communicating data using digital subscriber line (DSL) communications systems. Two main examples of these systems are Asymmetric DSL (ADSL) and Very-High-Bit-Rate DSL (VDSL). ADSL devices are also known as ADSL

transceivers or ADSL Transceiver Units (ATUs). There are two main types of ATUs: ATU-R at the remote or customer side, and ATU-C at the Central Office side. An ADSL connection consists of an ATU-C connected to an ATU-R using a phone line. In the case of ADSL, the ATU-C and the ATU-R comprise the communication endpoints. In the case of VDSL, the functionally equivalent units are known as VTU-C and VTU-R, at the central office side and at the remote or customer side.

13. Any communications system consists of three entities: transmitting entity, receiving entity, and channel entity. The transmitting entity and the receiving entity are on different sides of the channel entity. In the case of ADSL and VDSL these sides are also known as "CPE side" (Customer Premise Equipment side) and "CO side" (Central Office side). Communications channels have finite capacity and the data rates cannot be arbitrarily high.

14. ADSL equipment is capable of transmitting and receiving and, therefore, consists of a transmitting entity and a receiving entity. The transmitting entity and the receiving entity together comprise a transceiver. "[F]IG. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300." See A7 ('890 patent) at 4:41-43.

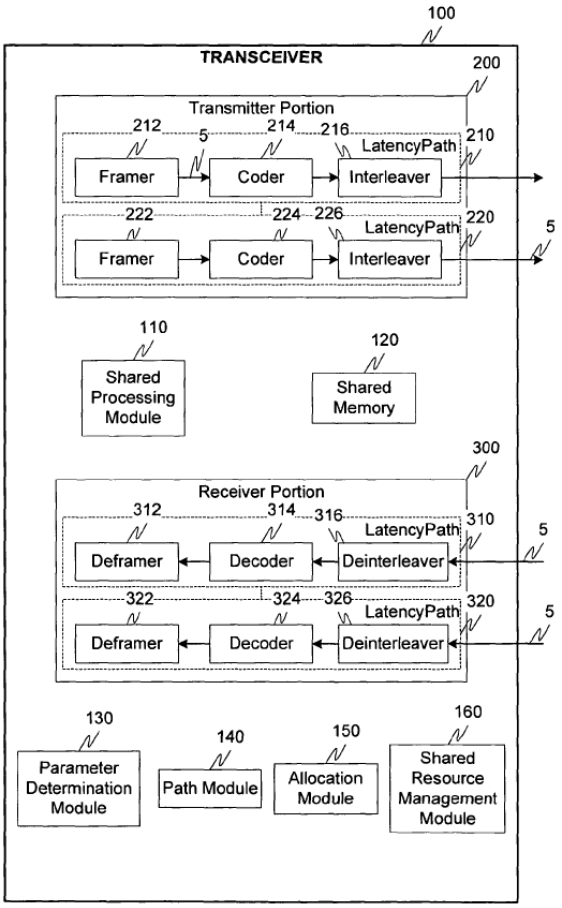
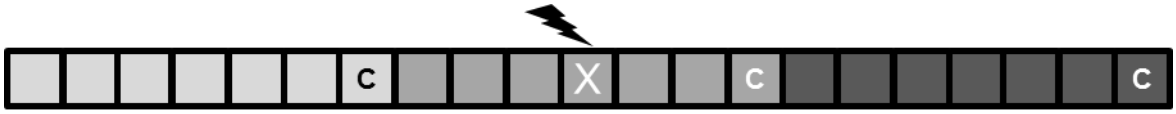


Fig. 1

A3 (‘890 patent) at Fig. 1.

15. In practical communications systems not all bits of data that are transmitted will be received correctly. Bits of data communicated over the communication medium may be corrupted by noise or interference. Noise is defined as “unwanted disturbances superimposed upon a useful signal that tend to obscure its information content.” A84 (IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, 7th ed. (2000) at p. 732). Thus, bits of data transmitted over a communication medium in the presence of noise may not be correctly received. Communications systems include a technique, typically based on Cyclic Redundancy Check (CRC), to determine if an error has taken place. If there has been an error, the data is re-transmitted. Specifically, to permit detection of errors caused by impulse noise or interference,

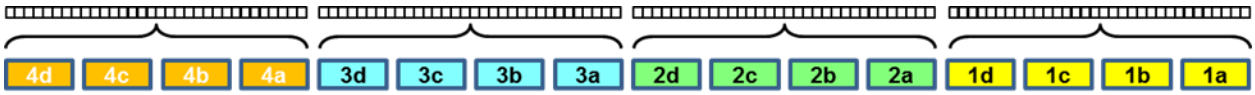
error detection bits, cyclic redundancy checksum ("checksum" or "CRC") bits for example, may be appended to groups of data bits before transmission. The transmitting end point may compute the checksum bits for the group of data bits and append it to the group of data bits prior to transmission. The figure below illustrates an exemplary bit stream that includes checksum bits 'C' for groups of data bits. Different shades of grey are used to differentiate the different groups of bits.



16. The receiving endpoint uses the checksum bits to confirm that respective groups of data bits were correctly received. For example, the receiving endpoint may independently compute the checksum for a group of data bits and compare the computed checksum with the checksum appended by the transmitting endpoint to the group of data bits. If the computed checksum matches with the appended checksum, the group of data bits was correctly received. Otherwise at least one of the data bits of the group was not correctly received, for example, because it was corrupted by impulse noise. In the example illustrated above, at least one data bit of the second group of bits is corrupted by impulse noise (marked with an 'X'). In this case the checksum computed for the second group of data bits will not match with the appended checksum computed by the transmitting endpoint.

17. Retransmissions are not generally desirable because re-sending the same data more than once reduces the effective data throughput. To reduce the negative impact of noise, error correction schemes may be used. The techniques that correct errors without the need for retransmissions are called Forward Error Correction (FEC). Use of Forward Error Correction causes latency (i.e., delay), but typically less delay than retransmission.

18. Use of Reed Solomon coding is one Forward Error Correction technique used with DSL systems. Reed-Solomon coding is a type of block coding. In Reed Solomon coding, groups of data bits may be encoded into corresponding sets of codewords prior to transmission. In place of the data bits themselves, the groups of data bits in each codeword are then transmitted sequentially over the communication medium. The encoding method used is one that allows a group of data bits to be recovered from its corresponding codeword. The figure below illustrates the groupings of data bits and the corresponding codeword generated from each group. Groups of bits and codewords would typically be communicated sequentially, for example as illustrated below, group 1a from codeword 1 being communicated first in time and group 4d from codeword 4 being communicated last in time:

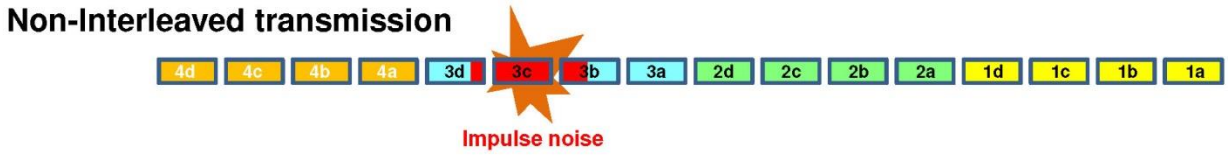


19. Reed-Solomon (RS) codes are block codes that operate over symbols of *s* bits each. The major parameters of RS codes are codeword length *n* and message length *k*. Coding involves two processes: encoding and decoding. Encoding is performed at the transmitter and decoding is performed at the receiver. The RS encoder takes *k* data symbols and adds *n-k* parity symbols to make a codeword of *n* symbols. This code is denoted as RS (*n, k*) and allows the decoder to correct up to *t* symbols that are erroneously received within one codeword, where $2t = n-k$. Thus, for any coding technique, including Reed Solomon, the size of a codeword is greater than the size of the data that the codeword encodes.

20. For example, the ITU-T recommendation for ADSL G.992.1 specifies that the number of parity bytes per RS codeword is 0, 2, 4, 6, 8, 10, 12, 14, or 16. For example, one RS code is RS (255, 239). This code operates using 8-bit symbols. Each codeword contains 255 bytes and consists of 239 message bytes and 16 parity bytes. The decoder can automatically (i.e.

without retransmission) correct up to *(n-k)/2*=8 bytes of errors. These 8 erroneously received bytes can be located anywhere among the 255 bytes of the codeword.

21. There are several types of noise. Thermal noise is always present. Thermal noise causes random bit errors. Another type of noise is impulse noise. Impulse noise that is defined as noise that is "characterized by transient disturbances separated in time by quiescent intervals." A82 (IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, 7th ed. (2000) at p. 732). One source of impulse noise is the switching of high-voltage electrical equipment. Impulse noise is intermittent and causes bursts of errors, i.e. consecutive errors (corrupted bits are shaded in red in the illustration below). If one or more bits from a codeword are corrupted by noise, the receiving endpoint may nevertheless be able to recover all of the original data bits using the portions of the codeword that are correctly received. To allow recovery of the original data bits from a codeword, a minimum or threshold number (or percentage) of bits from the codeword must be correctly received. If, however, more than a threshold number of bits from the codeword are corrupted by noise, the original data bits represented by a codeword will not be recoverable. This minimum or threshold number is a function of the level of encoding performed when translating the group of data bits to the codeword.



22. Because impulse noise involves short, intermittent bursts, a number of consecutive bits spanning one or more groups of bits in a codeword may be corrupted while other adjacent bits are received correctly (corrupted bits are shaded in red in the illustration above). If the duration of the impulse noise is sufficiently long, then more than a threshold number of bits of a codeword (for example, more than one quarter or 25% of the bits in a codeword) may be

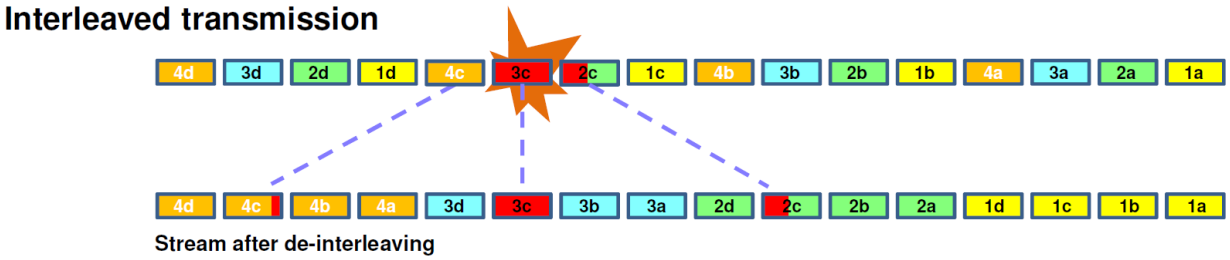
corrupted, which would make it impossible to recover the data bits corresponding to that codeword. In the example illustrated above, portions of (blue) codeword 3 (all of bits in group 3c and some of the bits of groups 3b and 3d totaling about 40% of the bits of the blue codeword) are corrupted by impulse noise. In this example where the threshold is 25%, it would be impossible to recover the original data bits that were used to generate (blue) codeword 3.

23. An improvement to the above-described error correction scheme spreads the impact of impulse noise across multiple codewords. This approach involves manipulating multiple codewords by rearranging the order in which groups of bits of the multiple codewords are transmitted. Groups of bits of a codeword, that otherwise would have been contiguous (i.e., transmitted sequentially), are rearranged so that once contiguous groups of bits of a codeword are now spaced further apart in time from each and interspersed with groups of bits from a number of other codewords. The process of rearranging the order in which groups of bits from multiple codewords are transmitted is called interleaving. Because impulse noise is relatively short in duration, spreading out portions of codewords in time ensures that any instance of impulse noise will tend to corrupt a smaller number of bits from any given codeword.

24. Upon receipt, the codewords are reassembled by rearranging the groups of bits back into their original order. The reverse process of reordering/reassembling the codewords to their original order is referred to as deinterleaving.

25. The illustration below depicts an interleaved data stream consisting of four groups of bits from four different codewords. In particular, the first groups of bits from the four different codewords (yellow #1a, green #2a, blue #3a, and orange #4a) is transmitted first; then a second group of bits from each codeword (yellow #1b, green #2b, blue #3b, and orange #4b) are transmitted and so on. As shown, impulse noise corrupts more than 25% of the total number of

bits in the third group of bits. However, once the data stream is deinterleaved so that the original codewords are reassembled, the effect of impulse noise is spread across multiple codewords and no individual codeword has more than 25% of its bits corrupted. This would allow the error correction code to recover all of the original data bits.

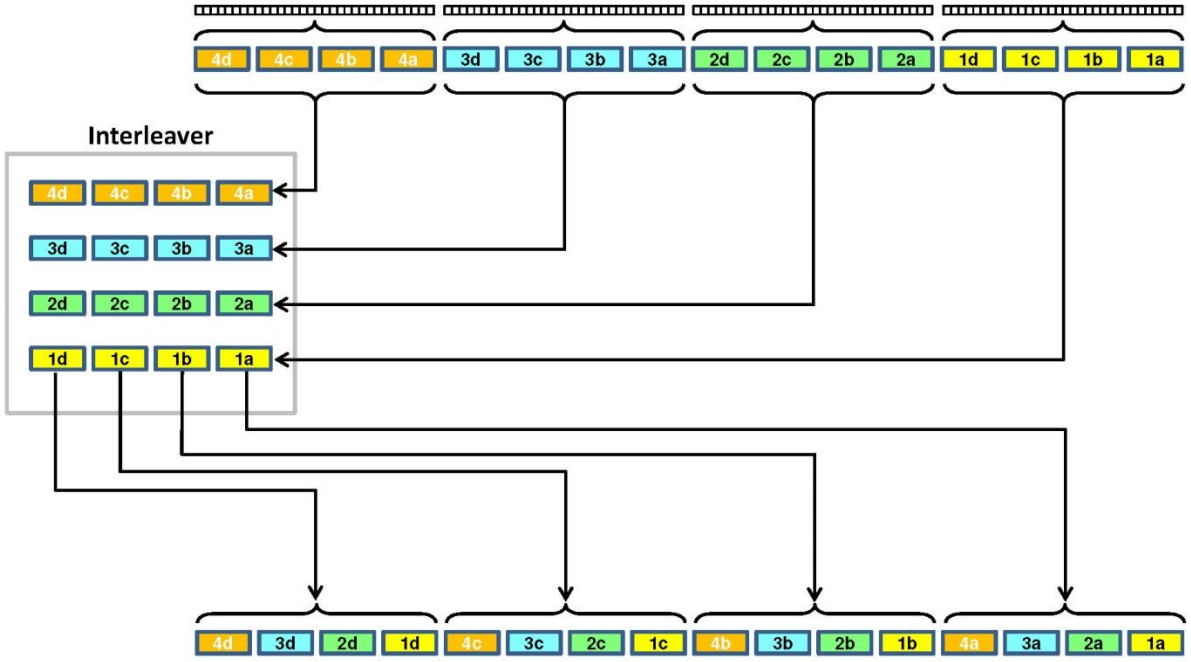


26. Latency is a very important parameter of communications systems. It includes the delay introduced by the protocol used to communicate the data. I will use the terms delay and latency interchangeably.

27. Interleaving increases throughput, because it reduces the need for retransmission. However, it has a downside because, as previously explained interleaving contributes to latency. This is because the entire interleaved block of multiple codewords must be received before deinterleaving and decoding can be performed. For example, in the illustration above, the first group of yellow bits (yellow #1a) must be stored while waiting for the second group (yellow #1b), third (yellow #1c), and fourth group (yellow #1d) of yellow bits to be received. Only after receipt of all of the bits of a codeword can the codeword be decoded. This delays the recovery of the original data bits. Similarly, on the transmitter side, the last of the codewords within an interleaved block of multiple codewords must be processed (e.g., encoded) before the first group of bits in the interleaved block can be transmitted. The time delay introduced because of the error correction and coding and interleaving/deinterleaving operation contributes to an increase in the overall latency. This increase in latency is a function of the number of bits in a codeword

(i.e., "codeword size") the number of codewords that are interleaved together (i.e., "interleaver depth"), and the data rate.

28. An interleaver is a component in a transceiver that accepts groups of bits of codewords and returns the identical groups of bits but in an order different from the order in which the groups of bits were received. An example of a simple interleaver is illustrated below in which each group of bits in each codeword is sequentially written into an interleaver memory row by row. The order of transmission of the groups of bits is then rearranged by reading out the groups of bits column by column.

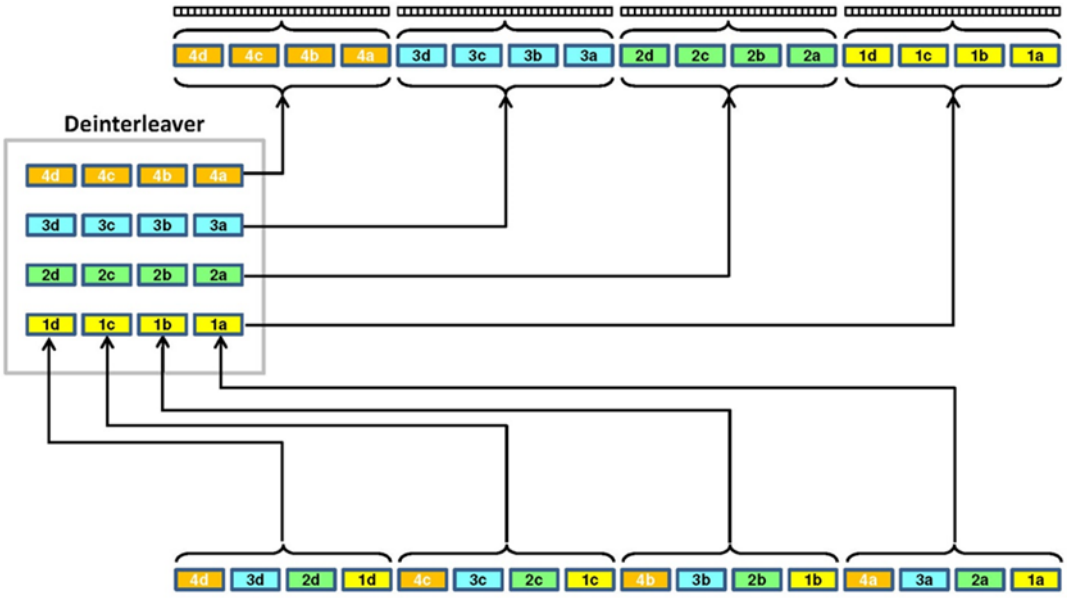


29. An important element of the interleaver is the interleaver memory that is used to perform the interleaving. As recognized by the Family 3 Patent specification, the size of the interleaver memory needed to perform the interleaving is determined by the number of codewords being interleaved together in one block (i.e., the interleaver depth), and the size of the individual codewords. Increasing the size of the block increases the error correction capability

of the system, but also increases the amount of memory required to perform the interleaving operation.

30. In the example above the depth of the interleaver is the number of codewords that are stored in the memory associated with the interleaver. One codeword of *n* symbols is written into each row of the interleave buffer. If the interleaver depth is D, the interleave buffer will be full after $n \cdot D$ symbol periods. If symbols occur every T seconds and the symbol rate is *1/T*, and one symbol contains *s* bits, then the data rate will be $R=s/T$ bits per second and the delay will be $n \cdot D/R$ seconds.

31. A deinterleaver is a component in a transceiver that receives a block of interleaved codewords, and reassembles the individual codewords of the block by rearranging the groups of bits of the codewords back into their original order. The deinterleaved codewords may then be decoded to recover the original data bits. An example of a simple deinterleaver is illustrated below. The received block of interleaved codewords is sequentially written into a deinterleaver memory column by column and rearranged by reading out the groups of bits row by row.



32. A transceiver includes a transmitter and a receiver. Consequently, such a transceiver

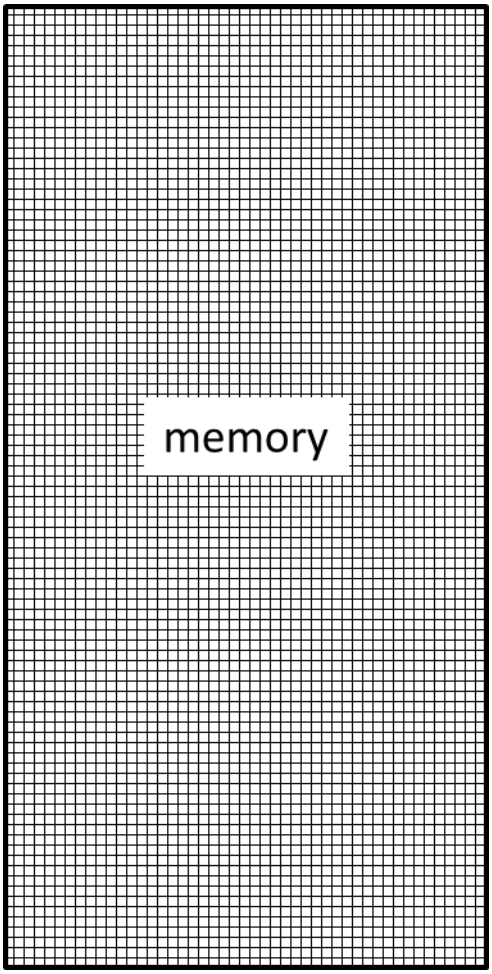
that uses interleaving and deinterleaving includes both an interleaver and a deinterleaver. The interleaver is used to interleave blocks of codewords prior to transmission and the deinterleaver is used to deinterleave received blocks of interleaved codewords.

33. Increasing the size of the block of codewords that are interleaved increases the error correction capability of the system, but also increases the amount of memory required by the system. The Family 3 patents recognize that when interleaving (and corresponding deinterleaving) are performed the amount of memory that is required by these functions is a very important consideration. Therefore, interleaving should not be used more than the minimum required to achieve acceptable performance.

34. As explained in the Family 3 Patent specification, the size of the individual codewords, Reed Solomon codewords for example, and the number of such codewords that are interleaved together determine the amount of the memory allocated to interleaving/deinterleaving that is actually used for the interleaving/deinterleaving operation. The Family 3 patents make clear that deinterleaving a block of codewords requires the same amount of memory as interleaving the same block of codewords. A8 ('890 patent) at 6:25-31 ("Reed Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R = 16) and interleaving/deinterleaving using an interleaver depth of 64(D=64). This latency path will require N*D = 255*64 = 16Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver).").

35. Memory is used to store information. A89-90 (IEEE Standard Dictionary of Electrical and Electronics Terms, 4th ed. (1988) at p 582 ("memory. See: storage") and p. 956 (defining storage as "[a]ny device in which information can be *stored*, sometimes called a memory device") (emphasis added)); see also A100-101 (Standard Dictionary of Computers and

Information Processing, Martin H. Weik, 3rd printing (1970) at p. 186 (stating that memory is same as storage) and p. 271 (defining storage as "a device . . . which receives data, holds and, at a later time, returns data."). Memory is comprised of memory cells. "A memory cell is the smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, or from which it can be retrieved." A83 (IEEE 100 The Authoritative Dictionary of IEEE Standard Terms, 7th ed. (2000) at p. 685 (defining memory cell as "the smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.") Shown below is an illustration of memory. Each cell of the grid corresponds to an exemplary memory cell.



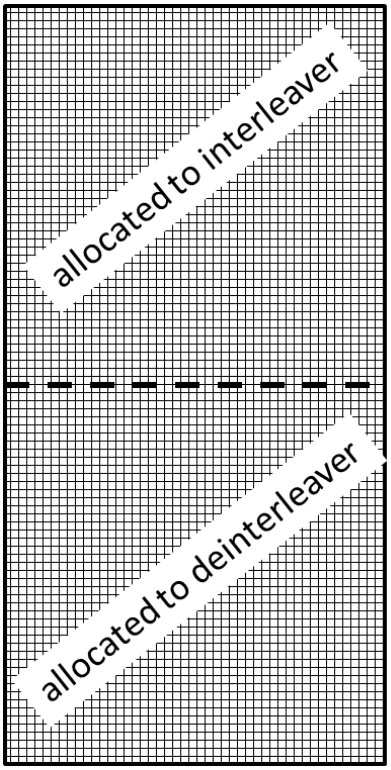
VI. The Family 3 Patents

36. The '890 patent recognizes that an interleaver and deinterleaver can consume a large amount of memory. *See* A6 ('890 patent) at 1:45-48 ("[A]n interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability.") The cost of memory can contribute significantly to the cost of DSL equipment.

37. Practical DSL transceivers are provided with a fixed amount of memory. Inventions described and claimed by the Family 3 Patents relate to "memory sharing in communication systems." A6 ('890 Patent) at 1:16-17. Specifically, the Family 3 Patents describe schemes to allocate shared memory between an interleaver and a deinterleaver of a transceiver. The interleaver and the deinterleaver of the transceiver each use all or a portion of its allocation of memory to perform interleaving and deinterleaving, respectively.

38. In the context of the Family 3 Patents shared memory is memory that can be allocated for use by one or more interleavers and one or more deinterleavers of a transceiver. *See* A6 ('890 Patent) at 1:57-59 ("[M]ore particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver."); A8 ('890 Patent) at 5:33-39 ("[F]or example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.") The figure below illustrates an example allocation of the shared memory between an interleaver and a deinterleaver. The portion of shared memory above the dashed line is allocated for use by the interleaver and the portion of shared memory below the dashed line is allocated for use by the deinterleaver. The interleaver uses memory cells from the portion of shared memory

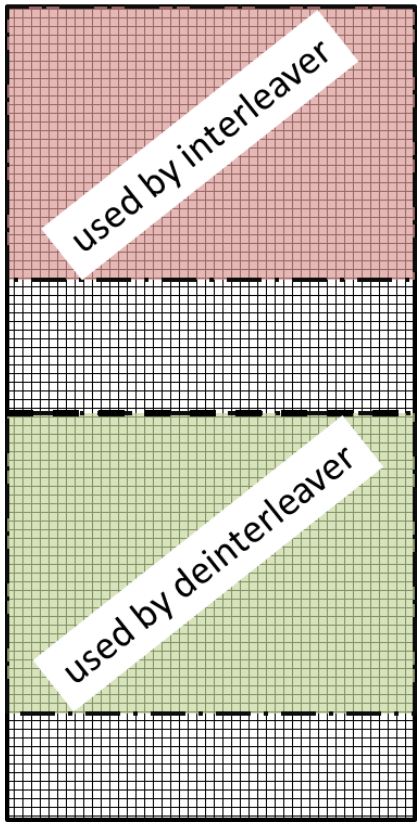
allocated to interleaving and the deinterleaver uses memory cells from the portion of shared memory allocated to deinterleaving.



39. The portion of the shared memory allocated to the interleaver can be used generally at the same time as the portion of the memory allocated to the deinterleaver. For example, the interleaver may be using a portion of the shared memory to store bits from codewords that are being interleaved at the same time that the deinterleaver is using a portion of the shared memory to store bits from codewords that are being deinterleaved. *See* A35 ('882 patent) at claim 13, 12:41-43 ("wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.")

40. The interleaver or deinterleaver may actually use less memory than the amount of shared membory allocated to the function. The figure below illustrates the allocation of shared memory used by the interleaver and the interleaver. The pink and green shaded areas of the

shared memory indicate the memory cells of the shared memory actually used by the interleaver and deinterleaver, respectively.



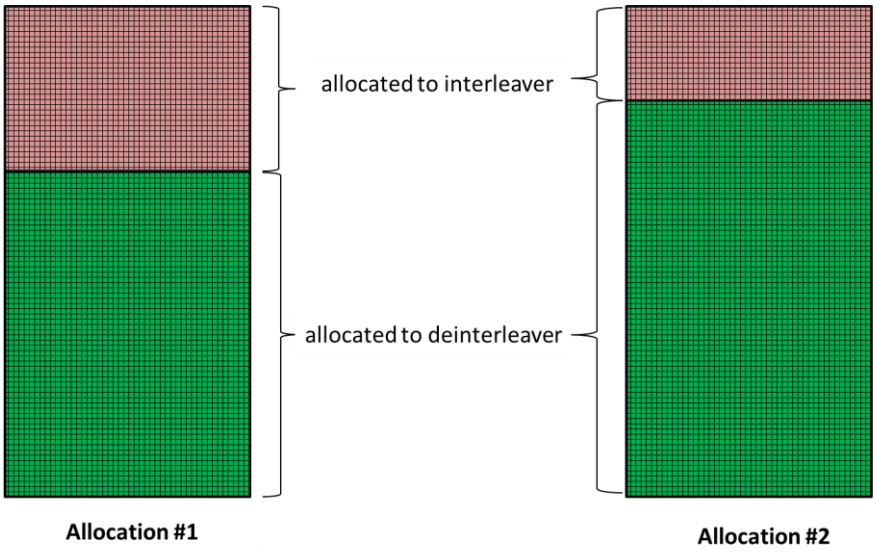
41. The sharing of resources such as memory requires some coordination between the two transceivers that form one DSL connection. To that end, the Family 3 Patents explain that the allocation may be performed after the transceivers exchange messages that "contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths." A7 ('890 Patent) at 4:23-28; *See also* A9 ('890 patent) at 8:47-51 ("[I]n this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings."). For example, based on the received messages, the transceiver may allocate a first portion of the

shared memory for use by an interleaver and allocate a second portion of the shared memory for use by a deinterleaver.

42. The Family 3 Patent specification explains that the allocation of shared memory between the interleaver and deinterleaver is not fixed. Instead, "the sharing of resources can be modified and messages transmitted between [] two transceivers at any time during initialization and/or user data transmission." A7 ('890 Patent) at 4:37-40. In other words, the messages exchanged between the transceivers are used to coordinate initial allocation, and any subsequent changes in the allocation, of shared memory. A9 ('890 patent) at 7:54-60 ("This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.").

43. The allocation may be adjusted in response to "a change in communication that would require the adjustment of the shared resource allocation." A10 ('890 Patent) at 9:29-32. "Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc." A10 ('890 Patent) at 9:32-34. The Family 3 Patent specification explains that applications like "video typically requires a low BER [bit error rate] (<1E-l0) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (> lE-3)." A6 ('890 Patent) at 1:27-30. Thus, if the traffic being handled changes from voice to video, the codeword size and the interleaving depth (together with the corresponding deinterleaving depth) may be increased to lower the bit error rate. This results in an increase in the memory size used by interleaving and its corresponding deinterleaving.

44. Within one transceiver, this may require a new allocation of memory so that portions of the shared memory that were previously used by the interleaver are now used by the deinterleaver. Thus, one or more memory cells that had been allocated to the interleaver may be used by the deinterleaver. Such a change in allocation is illustrated below. On the left (Allocation 1), a first allocation is shown with about 35% of the memory cells allocated to the interleaver and about 65% allocated to the deinterleaver. On the right (Allocation 2), a different allocation is shown with about 20% of the memory cells allocated to the interleaver and about 80% allocated to the deinterleaver. Per this example, about 15% of the memory cells that were at one time allocated to the interleaver are at another time allocated to the deinterleaver.



VII. The Disputed Claim Terms of the Asserted Patents

A. "transceiver" ('890 patent, claim 5, '381 patent, claim 5, '882 patent, claim 13, '048 patent, claim 1, '473 patent, claim 19, 28, and '126 patent, claims 1, 10)

45. In my opinion, this claim term is limited to a single device that is capable of transmitting and receiving. A "transceiver" is a well-understood term of art. Under the generally accepted definition, a transceiver is capable of transmitting and receiving and the transmitting

and receiving functions are implemented using at least some common circuitry. A78 (Hargrave's Communications Dictionary (2001) at p. 540); A96 (Merriam Webster's Collegiate Dictionary, 10th ed. (1993) at p. 1253) (defining transceiver as "a radio transmitter-receiver that uses many of the same components for both transmission and reception"); A91 (IEEE Standard Dictionary of Electrical and Electronics Terms, 4th ed. (1998) at p. 1028)(defining transceiver as "[t]he combination of radio transmitting and receiving equipment in a common housing, . . . , and employing common circuit components for both transmitting and receiving").

46. Because the transmitting entity and the receiving entity are part of a single device, they share some circuitry. For example, clock generation circuitry is typically shared. The sharing of elements between the transmitter and receiver is not done just out of convenience to reduce the cost of the device. DSL transceivers exchange messages. This message exchange would be more difficult if the transmitting and receiving entities were completely separate. In the context of the '890 patent, Figure 1 also indicates that the transmitting entity and the receiving entity of one transceiver share circuitry.

47. In contrast, the broad definition of "transceiver" proposed by Defendants could incorrectly be interpreted to include those types of designs where the transmitter is isolated from, and functionally unrelated to, the receiver (e.g., communicating using an entirely different communication scheme over a different medium) – something not contemplated by the patents-in-suit and the extrinsic evidence.

48. Therefore, a personal of ordinary skill in the art would understand a transceiver to be a "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry".

B. "shared memory" ('890 patent, claim 5, '381 patent, claim 5, '882 patent, claim 13, and '048 patent, claim 1)

49. I have reviewed Plaintiff TQ Delta's proposed construction for the term "shared memory" and agree that, particularly in view of the context provided by the patents, the terms means "a common memory space used by at least two functions, where particular memory cells within the common memory space can be used by either one of the functions"

50. I have also reviewed the Defendants' proposed construction of the term "shared memory". Defendants propose that the term means "single common memory in a transceiver used by at least two functions corresponding to at least two latency paths". This construction requires the memory to be single, which is unnecessary and technically inappropriate. The shared memory may be implemented using multiple separate and discrete blocks of memory. What is relevant is that the memory must be capable of being shared. Additionally, the phrase "single common memory" is ambiguous, at least because "single" could mean shared memory that is in a single semiconductor chip, a single memory module, or a single group of memory modules. Nevertheless, the patent specification does not restrict shared memory to a "single" physical object as Defendants seem to suggest.

51. Furthermore the construction proposed by the Defendants does not specify that the memory cells of this single common memory space can be used by either one of the functions, which is the definition of sharing. Additionally, Defendants' construction would include devices where a first function is restricted at all times to only using a first portion of a memory (e.g., a memory module) and a second function is restricted at all times to only using a second portion of the same memory. A person of ordinary skill in the art, upon reviewing the specification would recognize that an arrangement, where portions of the same memory are dedicated at all times to one function or the other, the memory is neither common to, nor shared by, the two functions.

See A7 ('890 Patent) at 4:37-40 ("the sharing of resources can be modified and messages transmitted between [] two transceivers at any time during initialization and/or user data transmission.").

C. "the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]" ('890 patent, claim 5, '381 patent, claim 5 '882 patent, claim 13, and '048 patent, claim 1)

52. Based on the parties' respective constructions, I understand that the parties disagree as to the meaning of the word "used" as it appears in the claims. Defendants seem to suggest that memory is "used" only when it is "read[] from or write[] to." This is an incorrect understanding of what it means to "use" memory. Memory is "any device in which information can be *stored*." A89-90 (IEEE Standard Dictionary of Electrical and Electronics Terms, 4th ed. (1988) at p 582 ("memory. See: storage") and p. 956 (defining storage as "[a]ny device in which information can be *stored*, sometimes called a memory device") (emphasis added)); see also A100-101 (Standard Dictionary of Computers and Information Processing, Martin H. Weik, 3rd printing (1970) at p. 186 (stating that memory is same as storage) and p. 271 (defining storage as "a device . . . which receives data, holds and, at a later time, returns data."). Thus, memory is primarily "used" to store or hold information. Defendants' construction does not account for this. TQ Delta's construction does. Therefore, this claim term properly construed means "information is stored in, read from, or written to the shared memory allocated to the deinterleaver at the same time that information is stored in, read from, or written to the shared memory allocated to the interleaver."

I declare under penalty of perjury that the foregoing is true and correct.

Dated: June 21, 2017

Dr. Todor Cooklev

Todor Cooklev, PhD.

Curriculum Vitae

Personal

1336 Sycamore Hills Parkway, Fort Wayne, IN 46814
Contact e-mail: tcooklev@gmail.com
Cell: 925-984-5283

Citizenship: United States (by naturalization)

Professional experience

Indiana University – Purdue University Fort Wayne, 2008 –

Founding Director, Wireless Technology Center, 2008 –

Harris Associate Professor of Wireless Communication and Applied Research, 2015 -

- Research on most aspects of wireless systems, including hardware, signal processing, and software techniques, in particular for software-defined radios.
- Endowed faculty appointment, Director of a Center of Excellence and appointment to the Purdue Graduate School
- Courses:
  ECE 428 Communication Systems
  ECE 549 Software-Defined Radio
  ECE 543 Wireless Communications and Networks

Consultant, Wireless Standards, 2005-2008, 2012.

- Voting Member, IEEE 802.11 WG; participated in the work on several 802.11 amendments
- Chair, IEEE 802.11 VTS Study Group; single-handedly proposed and won approval to create a Task Group that lead to the IEEE 802.11aa standard
- Attended meetings of the 3GPP RAN1 standardization committee in Dresden, Germany, Jeju Island, Korea, Prague, Czech Republic, and Qindao, China, 2012.

Datamars, Lugano, Switzerland, Consultant to the CTO, Wireless Standards, 2006-2008

- Evaluated and produced reports on certain wireless technologies and standards
- Participated in the IEEE 802.15.4f committee

Leica Geosystems, Switzerland, Consultant to the CTO, Wireless Standards, 2004-2006

- IEEE 802.16 (WiMAX) and related technologies

Doceotech, San Ramon, CA, Technical Advisory Board Member, 2005-2007.

San Francisco State University, 2002 – 2008, faculty with tenure (2008).

Aware, Inc., Lafayette, CA, 2000-2002, Member of the Technical Staff

- Worked on DSL standards. Participated in the International Telecommunications Union, Study Group 15, Question 4. Chaired the session on coding for DSL at the session in Antwerp, Belgium, June 2000
- Participated in the Telecommunications Industry Association T1E1 Committee on DSL
- Developed advanced coding for DSL
- Worked on the design of an IEEE 802.11a chipset.
- Voting member, IEEE 802.15; Co-Founder and First Vice-Chair of IEEE 802.15.3 (High-data rate wireless personal area networking

Quantronix, Framingham, Utah, Consultant, 1998-1999.

- Image processing; developed software for edge detection and wrote a report

Government of Canada, Communications Research Center, Consultant, 1996-1997.

- Designed digital filter banks for communication systems and wrote two technical reports

3Com Corporation, 1997-1999

- Worked on V.90 voice-band modems
- Implemented data compression and other signal processing algorithms V.42 and V.42bis
- Worked on the Bluetooth Standard, one of the first contributors to the Host Controller Interface of Bluetooth.
- Participated in the Bluetooth/IEEE group, which drafted the license agreement between Bluetooth and the IEEE 802, which in turn led to the establishment of the IEEE 802.15 Working Group.

Current expert witness engagements

- Evolved Wireless and TQ Delta, Austin, TX, 2015 -

Working with the law firm of Robins Kaplan as an expert on wireless communications involving the LTE standard on behalf of Evolved Wireless in connection with Civil Actions *No. 15-cv-542-SLR-SRF, No. 15-cv-543-SLR-SRF, No. 15-cv-544-SLR-SRF, No. 15-cv-545-SLR-SRF, No. 15-cv-546-SLR-SRF*, and *No. 15-cv-547-SLR-SRF (D-Del.)* brought against Apple, HTC, Lenovo, Samsung, ZTE, and Microsoft.

- TQ Delta, Austin, TX, 2014 -

Working with the law firm of McAndrews, Held & Malloy, Ltd. on behalf of TQ Delta as an expert on Digital Subscriber Line (DSL) modems and DSL technology in connection with Civil Actions *No. 1:14-cv-00954-RGA, No. 1:15-cv-00121-RGA* against Adtran*; No. 13-cv-1836-RGA* against Zhone Technologies Inc.; *No. 13-cv-2013-RGA* against Zyxel Communications Corporation, *No. 13-cv-1835-RGA* against 2Wire Inc, all filed in the United States District Court for the District of Delaware.

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Prior expert witness engagements

- Latham and Watkins, New York, NY, 2013-2015

Worked as an expert witness on behalf of Inter-Digital in connection with Civil Actions *No. 13-cv-00009-RGA* and *No. 13-cv-00010-RGA (D-Del.)* brought against ZTE and Microsoft Mobile Oy. For the purpose of infringement analysis wrote a 3G mobile phone application and server software. Produced six expert reports regarding infringement and validity of a patent pertaining to dual-mode 3G cellular/Wi-Fi devices and was deposed twice. Testified in front of the jury for infringement and validity at the ZTE trial, helping Inter-Digital win.

- Bunsow, De Mory, Smith, and Allison, San Francisco, CA, 2014-2015

Expert in wireless communications technology related to 2G cellular communication standards on behalf of Core Wireless Licensing, S.à.r.l. in connection with Civil Actions *No. 6:14-cv-752, No. 2:14-cv-911*, and *No. 2:14-cv-912 (E.D. Tex.)* brought against Apple, Inc. and LG Electronics, Inc.

- Dechert, Mountain View, California, 2014-2015

Expert in wireless communications and advanced coding as used in certain 2G GSM cellular communications standards in connection with Intellectual Ventures I LLC and Intellectual Ventures II LLC versus various AT&T, T-Mobile, Sprint, U.S. Cellular, and Cricket defendants (Civil Actions Nos. 13-cv-01668-LPS, 13-cv-01671-LPS, 13-cv-01670-LPS, 13-cv-01672-LPS, 13-cv-01669-LPS, 14-cv-01229-LPS, 14-cv-01230-LPS, 14-cv-01231-LPS, 14-cv-01232-LPS, 14-cv-01233-LPS)

- Kirkland & Ellis, San Francisco, CA, 2008-2010.

Worked as an expert on behalf of Intel in a matter brought by WiLAN and performed non-infringement and invalidity analysis of about twenty patents related to IEEE 802.16 (MAC/PHY/transmitter and receiver signal processing). Prepared and delivered a technology tutorial for the legal team at Kirkland & Ellis in San Francisco. Matter settled.

- Keker & Van Nest, San Francisco, CA, 2007-2008.

Worked as consultant on behalf of Intel Corp. in a matter brought by CSIRO. Performed non-infringement and invalidity analysis of a patent on coded OFDM and IEEE 802.11n.

Grants Awarded

1. NSF S^{2}ERC I/UCRC, "FPGA implementation of shared-memory middleware", 2017-2018, PI
2. NSF S^{2}ERC I/UCRC, "Shared-memory middleware", 2016-2017, PI
3. City of Fort Wayne, Economic Development Fund, 2013-15, co-PI.
4. Capital Improvement Board (CIB), 2013-15, co-PI, Power amplifier design for software-defined radios.
5. DARPA STTR Phase I "A flexible and extensible solution to incorporating new RF devices and capabilities into EW/ISR networks, co-PI, August 2013 – February 2014.
6. NSF S^{2}ERC I/UCRC, "The performance of middleware solutions for SDR", 2013-2014, PI
7. NSF S^{2}ERC I/UCRC, "Cognitive decision applications for embedded use," 2011-2012, PI
8. Visiting Fellowship, National Institute of Communication Technology (Japan), 2011
9. NSF S^{2}ERC I/UCRC, "Signal processing techniques for multicarrier modulation," 2009-2011, PI
10. NMDG, Belgium, laboratory grant 2010, PI
11. National Science Foundation, Professional Science Master's Program, MS in engineering, with concentration in wireless and systems engineering, 2010-2013, Co-PI.
12. Emona Instruments, Sydney, Australia, Laboratory exercises in communications, Principal Investigator, 2008.
13. Lilly Endowment, wireless laboratory grant, 2010, PI.
14. ITT (now Harris) Communications Systems, 2007-2011, PI.
15. State of Indiana, workforce development, 2008-2010, PI
16. NSF DUE-0442313, "Standards in Education for Product, Process, and Service Design and Development: A Proof-of-Concept Project," 2005-2008, PI.
17. France Telecom, Paris, France, "New methods for multicarrier modulation for high data-rate wireless systems," Principal Investigator, 2006.
18. Agilent Technologies/Sun Microsystems, Palo Alto, CA, "Distributed wireless sensor network for environmental monitoring," Co-principal Investigator, 2005.
19. CSU summer stipend, 2004.

20. U.S. Air-Force Research Laboratory, Wright-Patterson AFB, "Data over voice communications," Principal Investigator, 2004.

Honors and Awards

1) IEEE Standards Association, "for outstanding contributions to the development of IEEE 802.11aa", July 2012.
2) 2006 Wireless Educator of the Year Award with the citation "In recognition of the pivotal role of educators in preparing tomorrow's wireless technology leaders".
3) Duke's Choice Award, Sun Microsystems, 2005 (group award)
4) IEEE Communications Society Oakland/East Bay Chapter Achievement Award, 2003 (group award)
5) 3Com Inventor Award, 1999
6) NATO Science Fellowship Award, 1995-1997
7) IEEE Asia - Pacific Conference on Circuits and Systems Best Paper Award for the paper "Theory of filter banks over finite fields," Taipei, Taiwan, Dec. 1994.

Education

Tokyo Institute of Technology, Tokyo, Japan, Doctor of Philosophy in Electrical Engineering, 1995

Dissertation: Regular Perfect-Reconstruction Filter Banks and Wavelet Bases

Technical University of Sofia, Bulgaria, Dipl. Eng. in Electrical Engineering, 1988

Professional activities

Committee/Editorial Board Membership:
IEEE Communications Standards Magazine, Series Editor, Wireless and Radio Communications, 2017-

Committee Membership:

- IEEE 802.11 Working Group Voting Member, 2001-2003, 2006-present
- IEEE 802.15 Working Group Voting Member 1999-2001
- Chairman, IEEE Standards in Education Committee, 2006 – present
- Member of the Editorial Board, Journal of Networks.
- 2004-2005 Chairman and 2003-2004 Secretary of the Oakland/East Bay Chapter of the IEEE Communication Society.

Program Committee Membership:

- General Chair, Tactical Communications and Interoperability Conference, 2011
- General Chair, Fort Wayne Wireless Summer School 2009 and 2010
- Program Committee Member, Int. Conf. on Wireless Applications and Computing, 2007.
- Program Committee Member, Int. Conference on WLAN, WPAN, and WMAN, Hawaii, Aug. 2007.

- Program Committee Member, Int. Joint Conf. e-Business and Telecommunications, Barcelona, Spain, 2007.
- Program Committee Member, Int. Conf. Wireless Information Networks and Systems, Lisbon, Portugal, 2006.
- Technical Program Committee Member, Int. Conf. Networking and Services, ICNS 2006, Santa Clara, CA.
- Technical Program Committee Member, Advanced Int. Conference on Telecommunications, AICT, Guadeloupe, French Caribbean 2006.
- Program Committee Member, Int. Joint Conf. e-Business and Telecommunications, Reading, UK, 2005.
- Technical Program Committee Member, Int. Conf. Convergent Services and Next-Generation Networks, June 2005, Chicago, IL.
- Technical Program Committee Member, Int. Conference on Service Assurance with Partial and Intermittent Resources, Lisbon, Portugal, July 2005.
- Technical Program Committee Member, Int. Conf. Telecommunications, 2004, Brazil.
- 3rd Int. Workshop on Signal and Image Processing, Manchester, UK, Special session on wavelets in communication systems, signal and image processing, special session co-organizer, Nov. 1996.

Tutorials at International Conferences

1) T. Cooklev, "Open RF-digital interfaces and wireless ontologies," IEEE BlackSeaCom, 4th International Black Sea Conference on Communications and Networking, Varna, Bulgaria, June 2016.
2) M. Cummings, T. Cooklev, "Software Defined Radio Technology", Tutorial at the 2008 Symposium System on Chip, Tampere, Finland, Nov. 2008.
3) M. Cummings, T. Cooklev, "Software Defined Radio Technology", Tutorial at the IASTED Int. Conference Computer Communications, Palma de Mallorca, Spain, Sept. 2008.
4) M. Cummings, T. Cooklev, "Software Defined Radio Technology", Tutorial at the 2007 International Conference on Computer Design, Squaw Creek, CA 2007.
5) T. Cooklev, "Wireless communication standards: 802.11, 802.15, and 802.16," Int. Conference Telecommunications, Fortaleza, Brazil, Aug. 2004, tutorial.
6) T. Cooklev, "Wireless data communication standards, IEEE Globecom 2003, Dec. 2003, San Francisco, CA, tutorial.

Short Courses and Invited Talks excluding conferences:

1) T. Cooklev, "Modern Wireless Systems," Featured faculty presentation, Feb. 2012, IPFW.
2) T. Cooklev, "Software-defined radio technology," Tokyo Institute of Technology, Dec. 2011.
3) T. Cooklev, "Software-defined radio technology," University of Akron, OH, 2010.
4) T. Cooklev, "Modern wireless systems," University of Qatar, Doha, Qatar, 2009.
5) T. Cooklev, "Modern wireless systems," Technical University of Sofia, Bulgaria, 2009.
6) T. Cooklev, "Modern wireless systems: from Marconi's radio to cognitive radio," Sigma Xi presentation, February 2009, IPFW.
7) T. Cooklev "Software-Defined Radio Technology," Talk at IPFW, Oct. 2008.
8) M. Cummings, T. Cooklev, "Software Defined Radio Technology", IEEE Communication Society, Oakland/East Bay Chapter, presentation, Oct. 2007, San Ramon, CA.

9) T. Cooklev, “Engineering Standards in Engineering Education,” presentation and a panel participant, Standards Engineering Society Annual Conference, San Francisco, CA, August. 2007. (panelist and presenter)
10) T. Cooklev, “Vector transform for multicarrier modulation”, France Telecom, June 2007, Rennes, France.
11) T. Cooklev, “Wireless Communication Standards,” Distinguished Lecture, IEEE Communication Society, Oct. 2006, University of Maine.
12) T. Cooklev, “The IEEE 802.11, 802.15, and 802.16 Families of Standards,” Short Course, April 2006, Lietuvos Telekomas, Vilnius, Lithuania,
13) T. Cooklev, “The IEEE 802.11, 802.15, and 802.16 Families of Standards,” Short Course, Feb. 2006, Austin, TX.
14) T. Cooklev, “The IEEE 802.11, 802.15, and 802.16 Families of Standards,” Invited Talk, Dec. 2005, Cisco Systems, San Jose, CA.
15) Wireless local area networks, Hitachi Ltd., Brisbane, CA, June 2005.
16) T. Cooklev, “The IEEE 802.11, 802.15, and 802.16 Families of Standards,” Invited Talk, May 2005, Texas Instruments, Dallas, TX.
17) T. Cooklev, “Standards for the Wireless Internet”, IEEE Communication Society, Oakland/East Bay Chapter, presentation, January 2005. Freemont, CA.
18) T. Cooklev, “Wireless data communication standards, IEEE Wescon, Aug. 2003, San Francisco, CA, tutorial.
19) Short Course on 802.11, 802.15, 802.16, West Long Branch, NJ, August 2003
20) Wireless data communication standards, Lockheed Palo Alto Research Center, June 5, 2003.
21) Short Course on IEEE 802.11, 802.15, and 802.16, San Francisco, CA, Dec. 2002.
22) Standards for wireless data communications, University of Utah, Salt Lake City, UT, 1999
23) OFDM for wireless communications, 3Com Technology Forum, Boston, MA, Nov. 1998.
24) Filter banks and wavelets: a modern applied mathematics tool, Invited Lecture at the Analysis Day, Department of Mathematics and Statistics, Carleton University, Ottawa, Canada, 1997
25) Filter banks and wavelets for video signal processing, Genesis Microchip Inc, Markham, Ontario, Canada, July 1996.
26) Advanced topics in filter banks, wavelets, and their applications in modern communications systems, CRC, Ottawa, March and August 1996.
27) Digital filter banks and wavelets, Dept. Elect. Eng., University of Ottawa, March 1996.
28) Digital filter banks and wavelets, Dept. Elect. Eng., Queen's University, Kingston, March 1996.
29) Perfect-reconstruction filter banks and wavelet bases and their applications in digital communications, Fujitsu Laboratories, Kawasaki, Japan, July 1994.
30) Fast algorithms for signal processing, Istanbul University, Istanbul, Turkey, Jan. 1994.

M.S. students graduated

1. Farooq Khan, “Dynamic frequency selection and transmitter power control in 802.11,” 2002.
2. Xintong Li, “Throughput analysis and performance of 802.11e,” April 2003.
3. Stefano Iachella, “Deployment engineering of WLAN systems,” April 2003.
4. Chiya-yu Jin, “Packet-based FEC in wireless LAN,” Dec. 2003.
5. Amit Deshprabhu, “Comparison of 802.11a, 802.11b and 802.11g.” May 2004.
6. Vishal Shah, Throughput performance of IEEE 802.11 and IEEE 802.11e based Wireless Local Area Networks (WLAN), Jan. 2004.
7. Mario Goins, “System-on-a-chip for hardware minituarization of space flight systems,” 2004.

8. Qi Zhang, “Analyzing packet-based FEC in wireless LAN,” May 2004.
9. Yuhua Bai, “An improved lossless data compression method,” May 2004.
10. Chih-Kai Hsu, “Mobile security: enhanced RC4 algorithm,” Dec. 2004.
11. Huihui Zhang, “Throughput estimation of wireless mesh network,” January 2005.
12. Robert Chiu, “An energy efficient algorithm for wireless sensor networks.” Dec. 2004.
13. K. Rayment, “Wireless network system: Monitoring water flow with Hall effect sensors,”2005
14. K Thepsarn “Link adaptation simultaneously for slow and fast fading channels,” Dec. 2004.
15. Keh-Gang Lu, “A wavelet-transform based approach for the design sequences for communications”, Dec. 2004.
16. Afshaneh Pakdaman, “IEEE 1588 over IEEE 802.11b for synchronization of wireless local area nodes and DeviceNet,” May 2005.
17. Priya Santhana Vannan, “Data embedding in a GPS signal,” May 2005.
18. Yun (Jason) Chang, “Dynamic frequency selection and transmitter power control with smart antenna technology,” May 2005.
19. Shravai Vooturi, “Multicarrier modulation with vector transforms,” May 2005.
20. Lisseth Villareal, “Subband encoding of positional data over voice,” Nov. 2005.
21. Swaroopkanchan Karhale, “Evaluation of MICO and MIWCO for IEEE 802.11 wireless LANs,” Oct. 2005.
22. N. Munugeti, “An approach to reduce interference in coexisting collocated WPANs,” 2005.
23. Moitree Upadhaya, “Mobile ad-hoc networks,” June 2005.
24. Amey Khole, “Wireless sensor networks: network life extension via architecture modification,” Sept. 2005.
25. Adisak Manoprasertkul, ”Integration between wireless local area networks and 3G networks,” Dec. 2005.
26. Carlet Mesonge, “Dual-channel medium access control procedure,” Dec. 2005.
27. M. Keremane, “On the coexistence of different wireless personal area networks,” March 2006.
28. Deepthi Shetty, “Packet Sniffing,” May 2006.
29. Sathya Sekhar, “Implementation and performance of MIMO OFDM,” May 2006.
30. Ryan Jones, “Watermarking digital images using non-regular filter banks,” February 2006.
31. Yi-Chiya Liao, “Two-tiered sensor networks,” May 2006.
32. Wei Wang, “Cognitive radio approaches in wireless sensor networks,” May 2006.
33. Shalini Tripathi, “Smart Antenna Technology: Adaptive Algorithms Vs. Filter Banks: Reducing Interference in Wireless Communication Systems”, May 2006.
34. Henry Alvarez, “Contention window enhancements in EDCA,” May, 2007
35. Donovan Cheuk, “Performance of vector transform OFDM in the presence of carrier frequency offset,” May 2007.
36. Kuyng Tae Kang, “The fast vector transform algorithms and application to multicarrier communication systems,” June 2007.
37. Andrew Marcum, A Simplified Approach to Multi-Carrier Modulation, 2010.
38. Torrey Frank, A Generalized Prefix for Multi-Carrier Modulation, 2011.
39. David Clendenen, A Software Defined Radio Testbed for Research in Dynamic Spectrum Access, 2012.

Visiting Researchers

Dr. Fernando Ramirez-Mireles, Professor, ITAM, Mexico City, 2006.
Dr. Hakan Dogan, Associate Professor, University of Istanbul, Turkey, 2010.

Yusuf Acar, University of Istanbul, Turkey, 2011.

Publications

Books and Monographs

1) T. Cooklev, W*ireless communications standards: A Study of IEEE 802.11, 802.15, 802.16*, IEEE Press, New York, NY. 2004.

Chapters in Books

1) Subbu Ponnuswamy, Todor Cooklev, Yang Xiao, and Krishna Sumanth Velidi, "Security in fixed and mobile IEEE 802.16 networks," Chapter 4, *WiMAX/MobileFi: Advanced Research and Technology*, edited by Yang Xiao, Taylor and Francis, January 2008.

2) T. Cooklev and A. Hristozov, "The Software Communications Architecture," in *Resource Management in Future Internet*, edited by Ramjee Prasad, River Publishers, Denmark, 2015.

Journal Papers

1) H. Dogan, T. Cooklev, and J. Darabi, "Improved low-complexity zero-padded OFDM receivers", *Digital Signal Processing*, vol. 51, pp. 92–100, April 2016.

2) P. Baltiiski, I. Iliev, B. Kehaiov, V. Poulkov, and T. Cooklev, "Long-Term Spectrum Monitoring with Big Data Analysis and Machine Learning for Cloud-Based Radio Access Networks," *Wireless Personal Communications*, vol. 87, issue 3, pp. 815-835, April 2016.

3) T. Cooklev, J. Darabi, C. McIntosh, and M. Mosaheb, "Cloud-based approach for spectrum monitoring," *IEEE Instrumentation and Measurement Magazine*, vol. 18, no. 2, pp. 33-37, April 2015.

4) Sven Bilen, A. Wyglinski, C. Anderson, T. Cooklev, C. Dietrich, B. Farhang-Boroujeny, "On Software-Defined Radio as an integrative educational resource," *IEEE Communications Magazine*, vol. 52, no. 5, pp. 184-193, May 2014.

5) Hakan Yıldız, Yusuf Acar, Todor Cooklev, Hakan Dogan, "Generalized Prefix for Space-Time Block Coded OFDM Wireless Systems over Correlated MIMO Channels," *IET Communications*, vol. 8, no. 9, pp. 1589-1598, June 2014.

6) T. Cooklev, A. Nishihara, "An Open RF-Digital interface for software-defined radios," *IEEE Micro*, vol. 33, no. 6, pp. 47-55, Dec. 2013.

7) T. Cooklev, R. Normoyle, and D. Clendenen, "The VITA 49 RF-digital interface," *IEEE Circuits Systems Magazine*, vol. 12, no. 4, pp. 21-32, Dec. 2012.

8) T. Cooklev, “An improved prefix for OFDM-based cognitive radios”, *Electron. Lett.*, vol. 48, No. 4, Feb. 2012.

9) Y. Alqudah and T. Cooklev, “Hands-on open access broadband wireless technology lab”, *Int. J. Interactive Mobile Tech.*, Vol. 6, No 4, 2012, pp. 13-18.

10) T. Cooklev, H. Dogan, R. Cintra, H. Yildiz, “Generalized prefix for OFDM wireless systems over quasi-static channels,” *IEEE Transactions on Vehicular Technology*, vol. 60, No. 8, pp. 3684 – 3693, *Nov.* 2011.

11) F. Ramirez-Mireles, T. Cooklev, and G. A. Paredes-Orozco, “UWB-FSK: Performance tradeoffs for high-complexity receivers,” *IEEE Transactions on Consumer Electronics*, vol. 56, no. 4, pp. 2123-2131, 2010.

12) S. Hossain, D. Batovski, and T. Cooklev, “Eight-channel transmultiplexer with binary matrix sequences,” *Assumption Univ. Journal of Technology (Thailand)*, vol. 13, No. 4, pp. 193-202, 2010.

13) T. Cooklev, “Engineering standards and engineering education,” *Journal of IT Standardization Research*, vol. 8, 2010, pp. 1-10.

14) R. Cintra and T. Cooklev, “Robust image watermarking using non-regular wavelets,” *Journal of Signal, Image, and Video Processing*, 2008.

15) T. Cooklev, A. Pakdaman, J. Eidson, “IEEE 1588 over IEEE 802.11 for synchronization of wireless local area nodes,” *IEEE Trans. Instrumentation and Measurement*, Oct. 2007.

16) T. Cooklev and A. Nishihara, “Analytic constructions of complementary sequences,” *IEICE Trans. Fundamentals*, November 2006.

17) T. Cooklev, “An efficient architecture for orthogonal wavelet transforms,” *IEEE Signal Processing Letters*, Feb. 2006.

18) T. Cooklev, “Standards for the wireless Internet,” *Annual review of communications*, vol. 57, Dec. 2004.

19) T. Cooklev, G. Berbecel and A. N. Venetsanopoulos, ``Wavelets and differential-dilation equations,'' *IEEE Trans. Signal Processing*, vol. 48, pp. 2258-2268, 2000.

20) T. Cooklev and A. Nishihara, “Biorthogonal coiflets,”*IEEE Trans. Signal Processing*, vol. 47, pp. 2582-2588, 1999.

21) T. Cooklev, A. Nishihara, T. Yoshida, and M. Sablatash, ``Multidimensional two-channel linear phase FIR filter banks and wavelet bases with vanishing moments," *Journal of Multimensional Systems and Signal Processing*, vol. 9, pp. 39-76, January 1998.

22) T. Cooklev, A. Nishihara and M. Sablatash ``Regular orthonormal and biorthogonal wavelet filters," *Signal Processing*, vol. 57, pp. 121-137, Feb. 1997.

23) T. Yoshida, T. Cooklev, A. Nishihara, and N. Fujii, "Design of non-separable 3-D QMF banks using McClellan transformations," *IEICE Trans. Fundamentals*, vol. E79-A, No. 5, May 1996, pp. 716-720.

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UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC., Defendant.	Civil Action No. 13-cv-1835-RGA
TQ DELTA, LLC, Plaintiff, v. ZHONE TECHNOLOGIES, INC., Defendant.	Civil Action No. 13-cv-1836-RGA
TQ DELTA, LLC, Plaintiff, v. ZYXEL COMMUNICATIONS, INC., and ZYXEL COMMUNICATIONS CORPORATION, Defendants.	Civil Action No. 13-cv-2013-RGA
TQ DELTA, LLC, Plaintiff, v. ADTRAN, INC., Defendant.	Civil Action No. 14-cv-954-RGA
ADTRAN, INC., Plaintiff, v. TQ DELTA, LLC, Defendant.	Civil Action No. 15-cv-121-RGA

DECLARATION OF DR. KRISTA S. JACOBSEN IN SUPPORT OF DEFENDANTS' FAMILY 3 CLAIM CONSTRUCTION BRIEF

I. INTRODUCTION

1. My name is Krista S. Jacobsen. I have been asked by Defendants to provide this declaration in connection with the above-captioned District Court actions. Specifically, I have been asked to opine on the level of ordinary skill in the art at the time of the alleged invention, the state of the art at the time of the alleged invention, and how a person having ordinary skill in the art would have interpreted certain terms in U.S. Patent Nos. 7,831,890 ("the '890 patent"), 7,836,381 ("the '381 patent"), 7,844,882 ("the '882 patent"), 8,276,048 ("the '048 patent"), 8,495,473 ("the '473 patent") and 8,607,126 ("the '126 patent") (collectively, "the Family 3 Patents") at the time of the alleged invention. I have also been asked to opine on what I have identified as deficiencies of Dr. Todor Cooklev's declaration in support of TQ Delta's opening Family 3 claim construction brief.

II. BACKGROUND AND QUALIFICATIONS

2. I was awarded a Ph.D. in Electrical Engineering from Stanford University in 1996, and a Master's Degree in Electrical Engineering in 1993, also from Stanford University. I also hold a Bachelor of Science Degree in Electrical Engineering, *summa cum laude*, from the University of Denver, which I received in 1991.

3. My Ph.D. research focused on technology for digital communications, including multicarrier modulation, discrete multi-tone (DMT) modulation, and orthogonal frequency division multiplexing (OFDM). My doctoral thesis topic was "Discrete Multi-Tone-Based Communications in the Reverse Channel of Hybrid Fiber-Coax Networks." My research adviser was Dr. John M. Cioffi, who is known as the "father of DSL."

4. I am also a co-editor of two books on digital subscriber line (DSL) technology and the author of several book chapters on DSL technology and standardization. In addition, I have authored and co-authored numerous articles on multicarrier communications.

5. I have over ten years of experience working in the development and standardization of DSL technologies, including those embodied in the ITU-T Recommendations involved in the above-captioned District Court actions. I am an inventor named on eleven patents solving issues presented by or related to multicarrier modulation. My experience includes work in DSL technologies and the DSL industry both before and after the purported priority date of the Family 3 patents.

6. I am also licensed to practice before the Patent and Trademark Office. I am currently an attorney who serves as an expert consultant and witness for patent litigation, and I provide patent prosecution and counseling services in multiple areas, including telecommunications.

7. A detailed curriculum vitae showing more of my credentials is attached to this declaration as Appendix A.

III. COMPENSATION

8. I am being compensated for my time at the rate of $400 per hour. This compensation is not contingent on my performance, the outcome of this matter, or any issues involved in or relating to this matter.

IV. DOCUMENTS AND OTHER MATERIALS RELIED UPON

9. In forming the opinions set forth in this declaration, I have reviewed the asserted Family 3 patents and their file histories, including provisional application No. 60/618,269 ("the '269 provisional"). Additionally, I have considered my own experience and expertise concerning the knowledge of a person having ordinary skill in the relevant art during the timeframe of the claimed priority date of the Family 3 patents. I have reviewed information generally available to, and relied upon by, a person having ordinary skill at the time of the alleged invention. I have also reviewed TQ Delta's opening Family 3 claim construction brief

and Dr. Cooklev's declaration in support of TQ Delta's opening Family 3 claim construction brief.

10. I was told to assume the time of the alleged invention is October 12, 2004, the date on which the '269 provisional was filed.

V. LEGAL PRINCIPLES

11. Although I am licensed to practice law, I do not opine in this paper on any particular methodology for interpreting patent claims. My opinions are based on the meaning that a term would have had to a person having ordinary skill in the art in light of the specification and the prosecution history at the time of the filing of the '269 provisional on October 12, 2004. I am not opining in this paper as a patent expert; I applied the principles below, however, as a guide in formulating my opinions.

12. I am informed and understand that it is a basic principle of patent law that before the validity or infringement of a patent claim can be assessed, the claim language must be properly construed to determine its scope and meaning as understood by persons of ordinary skill in the art. I am informed and understand that the words of a patent claim are to be given the meaning that those words would have had to a person having ordinary skill in the art at the time of the invention in light of the specification and the prosecution history. This meaning must be ascertained from a reading of the patent documents, paying special attention to the language of the claims, the drawings, the written description, and the prosecution history of the Family 3 patents. I understand that an inventor may attribute special meanings to some terms by defining those terms or by otherwise incorporating such meanings in these documents.

13. I am informed and understand that for claim construction, intrinsic evidence is more important and considered more reliable than extrinsic evidence. Consequently, where possible, I have relied primarily on intrinsic evidence in forming my opinions. Where I found

the intrinsic evidence to be lacking, I relied on my experience as a person who worked in the DSL field at the time of the alleged invention, as well as DSL standards that would have been known to persons having ordinary skill in the art.

14. My methodology for determining the meaning of claim terms and phrases was first to study the Family 3 patents. In particular, I studied the claims themselves, the written description (which includes the background, the summary, and the detailed description of the invention), and the drawings. Next, I reviewed the file histories of the Family 3 patents, looking for any clarifications of or limitations that might be attached to claim terms. In some circumstances, I looked at other documents, such as references applied by the U.S. Patent and Trademark Office, provisional applications to which applications claimed priority, or documents incorporated by reference or referenced in the Family 3 patents.

VI. LEVEL OF SKILL IN THE ART

15. I disagree with Dr. Cooklev's characterization of the level of skill a person having ordinary skill in the art would have had on October 12, 2004. In my experience, at that time, a person having ordinary skill in the art would have had a bachelor's degree in electrical or computer engineering and 5-6 years of experience, a Master's degree in electrical engineering and 2-3 years of experience, or a Ph.D. in electrical engineering with 1-2 years of experience.

VII. BACKGROUND OF THE TECHNOLOGY

16. I agree with much of Dr. Cooklev's explanation of error detection, forward error correction, interleaving, and deinterleaving. Cooklev Dec. at ¶¶ 15-32. These techniques were well known at the time of the alleged invention and had been in use long before the priority date. For example, by 1993, forward error correction using Reed-Solomon coding in conjunction with interleaving and cyclic redundancy check (CRC) bytes had been incorporated into the draft of the original T1.413 standard for ADSL. *See, e.g.*, A223, A248-49 ("Asymmetric Digital Subscriber

Line (ADSL) WORKING DRAFT Standard" (T1E1.4/93-007), §§ 6.2.1, 7.2.1 ("Up to four downstream simplex data channels and up to three duplex data channels are multiplexed and synchronized to the 4 kHz ADSL DMT symbol rate into two separate data buffers (fast and interleaved). A cyclic redundancy check (crc), scrambling, and forward error correction (FEC) coding are applied to each data buffer separately. The interleaved data buffer is then passed through an interleaving function."); A235 (T1E1.4/93-007), § 6.4. (describing use of Reed-Solomon coding); A259 (T1E1.4/93-007), § 7.4.1 (same).

17. Furthermore, the tradeoffs between error correction capability and latency were also well known well before the priority date of the Family 3 patents, as was the delay inherent in interleaving/deinterleaving. The earliest ADSL standard, T1.413-1995, included mechanisms enabling the transport of both delay-sensitive traffic (using a "fast," or low-latency, data buffer) and traffic that could tolerate more delay (using an "interleave" data buffer). *See, e.g.*, A352 (T1E1.4/95-007R2 § 5.4) (referring to "synchronization control for the bearers transported with interleaving delay (interleave data buffer) and with no interleaving delay ('fast', or low-latency, data buffer)"). Likewise, the first version of the ITU-T's ADSL Recommendation, G.992.1, specified both fast and interleaved paths and stated that "the 'fast' path provides low latency; the interleaved path provides very low error rate and greater latency." A580 (G.992.1 (06/99) at § 5.1.1).

18. Thus, to the extent the Dr. Cooklev has presented error detection, error correction, and interleaving/deinterleaving as if they were points of novelty of the alleged invention(s), I disagree with that presentation.

VIII. FAMILY 3 PATENTS

19. I disagree with certain aspects of Dr. Cooklev's characterizations of the Family 3 patents.

A. Sharing Memory Between Latency Paths and Between Interleavers and Deinterleavers Was Well Known to Skilled Artisans and Was Not Novel At the Time Of the Alleged Invention.

20. At the time of the alleged invention, sharing memory between interleavers, deinterleavers, and latency paths in transceivers was well known in the art. Before the purported priority date, sharing memory between two latency paths of a transceiver had been discussed at standards meetings. *See, e.g.*, A532 (ITU-T SG15/Q4 contribution LB-041), item 11.8 (indicating that ETSI TM6 (the group of the European Technical Standards Institute responsible for DSL standardization) had observed that "Interleaver memory could be shared between the two [latency] paths and the aggregate delay of the two paths need not exceed 20ms").

21. I have reviewed the prosecution history of the '890 patent. I understand that the Examiner located a reference, U.S. Patent No. 6,707,822 to Fadavi-Ardekani *et al.* (hereinafter, "Fadavi-Ardekani"), that discloses sharing memory between an interleaver and deinterleaver. *See, e.g.*, A616 (Fadavi-Ardekani), 5:57-6:6 ("The Frame Buffer (FB) 224 provides a dual access memory that is used in a ping-pang fashion. . . . 'Ping-pang' means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of memory is being used by a first agent, another area of memory can be used by a different agent. As long as different agents (in this case, the ATM accelerator and the FCI) access different areas of a dual access memory, there are no memory address conflicts that could cause communication errors. At any time, an agent is allowed to access either a ping area of memory or a pang area of memory based on the logic level of the virtual clock signal. Thus, the FB should be allocated a memory of a size sufficient to provide ping-pang functionality."); *id.*, 6:55-65 ("The Interleave/De-Interleave Memory (IDIM) 230 provides a memory through which the FCI 226 interfaces the DSP core 228. The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion. The IDIM is used to transfer

framed, coded and possibly interleaved data frames between the FCI core and the DSP Core. In addition to interleave data storage, the IDIM may contain a dedicated area for the transfer of fast path data to the DSP Core. The IDIM may be organized as 16 bit words with byte write capability to allow beneficial performance of various interleave/de-interleave processes."); A617 (Fadavi-Ardekani), 7:25-30 ("An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path)."); *id.*, 8:62-65 ("the DSP core may load new DMT frames of [receive] data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory.") (emphases added).

22. Thus, to the extent the Dr. Cooklev has presented memory-sharing between an interleaver and a deinterleaver or between latency paths as if it were a point of novelty of the alleged invention(s), I disagree with that presentation.

B. The Family 3 Patents Do Not Disclose "Memory Cells."

23. In both the "Background of the Technology" and "The Family 3 Patents" sections of his declaration, Dr. Cooklev refers to "memory cells." *See, e.g.*, Cooklev Dec. at ¶¶ 35, 38, 40, 44. But the specification, claims, and prosecution history of the Family 3 patents never once use the term "memory cell(s).".

24. Furthermore, a person having ordinary skill in the art at the time of the alleged invention would not have referred to "memory cells" in the context of the Family 3 patents, which present the alleged invention as applied to DSL. A7 ('890 patent), 3:12-15. A skilled artisan would have understood interleaver/deinterleaver memory in DSL as being characterized by a size specified by a number of bytes, particularly because standardized aspects of DSL having to do with the interleaver/deinterleaver are specified or measured in bytes. *See, e.g.*,

A574 (G.992.1 (06/99), § 3.10 (defining data frame as "[a] grouping of bytes from fast and interleaved paths over a single symbol time period after addition of FEC bytes and after interleaving"); A575 (G.992.1 (06/99), § 3.19 (defining FEC output data frame as "[t]he grouping of bytes from fast or interleaved path over a single symbol time period after addition of FEC bytes and before interleaving"); § 3.22 (defining mux data frame as "[t]he grouping of bytes from fast or interleaved path over a single symbol time period before addition of FEC bytes and before interleaving"); *id.*, § 3.33 (defining sync byte as "[a]n overhead byte present at the beginning of each mux data frame (called 'fast' byte in the fast path and 'sync' byte in the interleaved path)"); § 4 (defining variable B_I as "[t]he number of bytes per frame in a data stream allocated to the interleaved buffer," K_I as the "[n]umber of bytes in a downstream (or upstream) interleaved mux data frame," N_I as the "[n]umber of bytes in a downstream (or upstream) FEC output-interleaved data frame," and R_I as the "[n]umber of downstream (or upstream) FEC redundancy bytes for interleaved buffer"); A599 (A574 (G.992.1 (06/99), § 7.4.1.2 (stating that "bytes of the fast data buffer shall be clocked into the constellation encoder first, followed by the bytes of the interleaved data buffer."); A601-02 (A574 (G.992.1 (06/99), § 7.4.1.2.2 (specifying frame structure for interleaved data buffer in bytes, and stating that "The interleaving process (see 7.6.3) delays each byte of a given FEC output data frame a different amount") (emphases added). Likewise, other key aspects of the framing of data in ADSL are also specified in bytes. *See, e.g.*, *id.* at § 6.3 (indicating ADSL uses CRC bytes, FEC redundancy bytes, and synchronization control bytes); A597-98 (G.992.1 (06/99), § 7.4.1.1, FIG. 7-5 (illustrating that ADSL superframe for ATU-C specified in bytes); A601-02 (A574 (G.992.1 (06/99), § 7.4.1.2.2 (illustrating interleaved data buffer specified in bytes and indicating that FEC codeword lengths are specified in bytes); A608 (G.992.1 (06/99),§ 7.6 (specifying FEC in terms of bytes).

25. Thus, at the time of the alleged invention, in view of the Family 3 patents' specification and its presentation of the alleged invention in the context of DSL, a person having ordinary skill in the art would have referred to memory in terms of bytes, not "memory cells."

IX. DISPUTED CLAIM TERMS

A. "transceiver"

26. In my opinion, a person having ordinary skill in the art at the time of the alleged invention would have understood "transceiver" to mean "communications device capable of transmitting and receiving data" as Defendants propose.

27. When looking at the Family 3 patents' specification, a person having ordinary skill in the art at the time of the alleged invention would not have understood that "the transmitter portion and receiver portion share at least some common circuitry." The Family 3 patents do not include any written description or drawings to indicate that a transceiver includes common circuitry shared by its transmitter and receiver portions.

28. Dr. Cooklev contends that "Figure 1 also indicates that the transmitting entity and the receiving entity of one transceiver share circuitry." Cooklev Dec. at ¶ 46. But FIG. 1 shows a transmitter portion 200 with a framer, coder, and interleaver for each latency path, and a separate receiver portion 300 with a deframer, decoder, and deinterleaver for each latency path. Nothing in FIG. 1 or elsewhere in the Family 3 patents would have suggested to a person having ordinary skill in the art at the time of the alleged invention that the transmitter portion 200 and the receiver portion 300 include shared circuitry; indeed, FIG. 1 illustrates them as separate blocks.

29. FIG. 1 also illustrates various "modules" within the transceiver 100, but nowhere do the drawings or the specification indicate that such modules are circuitry, and the specification states explicitly that "[t]he term module as used herein can refer to any known or

later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element." A7 ('890 patent), 3:50-53. Thus, all of the various modules illustrated in FIG. 1 may be realized entirely in software, which means they are not "common circuitry" to one having ordinary skill in the art.

30. The dictionary definitions Dr. Cooklev cites, all of which include the term "radio," appear to be definitions specific to wireless transceivers. Cooklev Dec. at ¶ 45. In contrast, the Family 3 patents describe the alleged invention in the context of DSL. *See, e.g.*, A7 ('890 patent), 3:12-15. Because the design constraints (*e.g.*, power, size, etc.) for wireless transceivers differ from those for DSL transceivers, the definitions Dr. Cooklev cites would not have been considered controlling by a person having ordinary skill in the art of DSL.

31. Although the transmitter and receiver of a transceiver *can* share common circuitry, a person having ordinary skill in the art on the presumed priority date would not have understood shared common circuitry to be an inherent characteristic or a requirement of transceivers. Dr. Cooklev admits that shared circuitry is not a requirement of a transceiver. *See* Cooklev Dec. at ¶ 46 ("clock generation circuitry is *typically* shared. . . . DSL transceivers exchange messages. This message exchange *would be more difficult* if the transmitting and receiving entities were completely separate.") (emphasis added). But Dr. Cooklev does not identify anything in the Family 3 patents that requires or even suggests that the claimed transceivers necessarily share common circuitry.

32. In my opinion, the "common circuitry" requirement would introduce confusion into the term, because a person having ordinary skill in the art at the time of the alleged invention would not have known how much circuitry would have to be "common" in order to meet the claim. In addition, Dr. Cooklev's and TQ Delta's concern that without the "common circuitry"

limitation, a transceiver could include wholly unrelated communications systems is unfounded. A skilled artisan would have understood that a "communications device" would not include systems that are entirely independent from one another.

33. Consequently, in my opinion, based on the disclosures in the Family 3 patents, a person having ordinary skill in the art at the time of the alleged invention would have understood a transceiver to be simply a "communications device capable of transmitting and receiving data" as Defendants have proposed.

B. "shared memory"

34. In my opinion, a person having ordinary skill in the art at the time of the alleged invention would have understood "shared memory" to mean "single common memory in a transceiver used by at least two functions corresponding to at least two latency paths" as Defendants propose.

35. Dr. Cooklev asserts, without any citation to intrinsic or even extrinsic evidence, that "[t]he shared memory may be implemented using multiple separate and discrete blocks of memory." Cooklev Dec. at ¶ 50. The Family 3 patents do not support Dr. Cooklev's assertion. The written description repeatedly refers to the shared memory as a singular object. *See, e.g.*, A8 ('890 patent), 5:18-23 ("a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120. . . . The interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers."); *id.*, 5:33-39 ("an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.") (emphases added). *See also id.*, 5:40-46; *id.*, 5:47-57; A9

('890 patent), 7:9-11 (repeatedly referring to "the" shared memory). Furthermore, despite the specification's inclusion of an entire column of boilerplate language attempting to sweep in implementation possibilities for myriad "wired and/or wireless telecommunications devices . . . capable of implementing the methodology illustrated herein," A10, ('890 patent), 9:38-10:36, not once does the specification state that the shared memory may be a collection of "multiple separate and discrete blocks of memory" as Dr. Cooklev contends.

36. A person having ordinary skill in the art would also understand the surrounding claim language in the Family 3 patents to require "a single common memory." Each of the asserted claims in which this term appears refers only to "a" or "the" shared memory, which implies that there is only one single memory. *See* A11 ('890 patent), claim 5; A23 ('381 patent), claim 5; A35 ('882 patent), claim 13; A47 ('048 patent), claim 1.

37. Furthermore, although Dr. Cooklev contends that the shared memory may be implemented "using multiple separate and discrete blocks of memory," he does not explain what he means by "blocks of memory." Cooklev Dec. at ¶ 50. Dr. Cooklev criticizes Defendants' proposed construction as allegedly extending to "shared memory that is in . . . a single group of memory modules." *Id.* at ¶ 51. A person having ordinary skill in the art at the time of the alleged invention could well have considered a group of memory modules to be "multiple separate and discrete blocks of memory," and therefore it is unclear what physical element or elements Dr. Cooklev believes constitute "shared memory."

38. TQ Delta's proposal of "a common memory space used by at least two functions, where particular memory cells within the common memory space can be used by either one of the functions" is ambiguous at least because it is unclear what constitutes "a common memory space." A person having ordinary skill in the art at the time of the alleged invention would not

have known whether a common memory space means the physical storage locations of a memory—*i.e.*, hardware—or a collection of software addresses, corresponding to and identifying physical storage locations, that are divorced from the physical memory implementation. Coupled with Dr. Cooklev's assertion that "[t]he shared memory may be implemented using multiple separate and discrete blocks of memory," TQ Delta's proposal introduces confusion in the construction of the term "shared memory" because it is unclear whether a "common memory space" refers to software or hardware. In contrast, Defendants' construction states that a single common memory, which a person having ordinary skill in the art would have recognized as hardware, is "used by"—and thus, shared by—at least two functions corresponding to at least two latency paths. This is also consistent with the contemporaneous understanding of the term "shared memory" to a person having ordinary skill in the art. *See* A556 (2004 Oxford University Press Dictionary of Computing, p480) (defining shared memory as "The use of the same portion of memory by two distinct processes, or the memory so shared. Shared memory is used for interprocess communication and for purposes, such as common subroutines, that lead to compactness of memory.")

39. TQ Delta's proposed construction is also amenable to the same interpretation for which Dr. Cooklev criticizes Defendants' proposal, namely that it "would include devices where a first function is restricted at all times to only using a first portion of a memory (e.g., a memory module) and a second function is restricted at all times to only using a second portion of the same memory." Cooklev Dec. at ¶ 51. TQ Delta's proposal specifies only that "*particular* memory cells within the common memory space can be used by either one of the functions"—it does not specify that *every* memory cell within "the common memory space" (whatever that is) can be used by either one of the functions. Thus, TQ Delta's proposal would extend to

arrangements in which portions of "the common memory space," which Dr. Cooklev contends may include multiple separate and discrete blocks of memory, are always used by the interleaver or by the deinterleaver. This arrangement would be inconsistent with Dr. Cooklev's opinion that "where portions of the same memory are dedicated at all times to one function or the other, the memory is neither common to, nor shared by, the two functions." *Id.*

40. Furthermore, there is nothing in the Family 3 patents that supports TQ Delta's reading of "memory cells" into the claims, particularly when the term "memory cells" is not used anywhere in the patents. Moreover, as explained above, like the Family 3 patents, a person having ordinary skill in the art at the time of the alleged invention would have referred to memory used in DSL in terms of bytes, not memory cells.

41. Thus, it is my opinion that a person having ordinary skill in the art at the time of the alleged invention would have understood "shared memory" to mean "single common memory in a transceiver used by at least two functions corresponding to at least two latency paths."

C. "amount of memory"

42. In my opinion, a person having ordinary skill in the art at the time of the alleged invention would have understood "amount of memory" to mean "number of bytes of memory" as Defendants propose.

43. Asserted claim 5 of the '890 patent recites:

> 5. A method of allocating shared memory in a transceiver comprising:
> transmitting or receiving, by the transceiver, a message during initialization specifying a maximum **number of bytes of memory** that are available to be allocated to a deinterleaver;
> determining, at the transceiver, **an amount of memory** required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data **bytes within a shared memory**;

> allocating, in the transceiver, a first **number of bytes of the shared memory** to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum **number of bytes** specified in the message;
> allocating, in the transceiver, a second **number of bytes of the shared memor**y to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate; and
> deinterleaving the first plurality of RS coded data **bytes within the shared memory** allocated to the deinterleaver and interleaving the second plurality of RS coded data **bytes within the shared memory** allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

A11 ('890 patent), claim 5 (emphasis added).[1] All of the other asserted claims that recite "amount of memory" contain similar disclosures that likewise *only* refer to "bytes." *See id.*, , claim 5; A35 ('882 patent), claim 13; A47 ('048 patent), claim 1. Thus, the claim language supports Defendants' proposed construction.

44. Similarly, the Family 3 patents' written description only discusses amounts of memory in terms of bytes. For example, the Summary explains that "a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver." A6 ('890 patent), 1:48-50. Furthermore, every example in the written description specifies quantities of memory in terms of bytes. *See, e.g., id.* at A8 ('890 patent), 6:29-31 ("This latency path will require N*D=255*64=16Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver).") (emphasis added); *id.*, 6:42-45 ("This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory.") (emphasis added); *id.*, 6:57:60 ("According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency

[1] Claim 5 is reproduced as corrected by the certificate of correction.

paths that share one memory space containing at least (16+4)=20 Kbytes.") (emphasis added); A9 ('890 patent), 7:16-22 ("Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes.") (emphasis added); *id.*, 7:34-46 ("Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. . . . Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example.") (emphasis added); *id.*, 8:15-19 (specifying maximum and total interleaver memory amounts in kbytes); *id.*, 8:29-30 (total interleaver memory is 20 kbytes); *id.*, 8:38-39 (same).

45. Defendants' proposed construction is also consistent with usage in the field at the time of the alleged invention. For example, as explained above, in paragraph 24, DSL standards in existence at the time of the alleged invention specify interleaver and deinterleaver requirements in terms of bytes, not "memory cells" or bits.

46. The Family 3 patents do not use "bit" as a measure of an amount of memory. Instead, the Family 3 patents discuss quantities of memory in terms of bytes. The patents' use of the conventional units of memory makes sense given their reliance on, and purported applicability to, DSL, which specifies interleaver/deinterleaver requirements in terms of bytes.

47. Thus, it is my opinion that a person having ordinary skill in the art at the time of the alleged invention would have understood "amount of memory" to mean "number of bytes of memory."

D. "the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]"

48. In my opinion, a person having ordinary skill in the art at the time of the alleged invention would have understood "the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]" to mean "the deinterleaver/interleaver reads from or writes to its respective allocation of the shared memory at the same time as the interleaver/deinterleaver reads from or writes to its respective allocation of the shared memory."

49. I did not find the phrase "at the same time" anywhere in the written description or drawings. Nevertheless, Defendants' proposed construction is consistent with how a person having ordinary skill in the art at the time of the alleged invention would have understood the written description, which discloses that "the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path." A7 ('890 patent), 4:1-13; *see also id*., 4:57-65.

50. TQ Delta's proposed construction would characterize portions of the shared memory *previously written* by an interleaver/deinterleaver as being "used at the same time" as memory actively being written to or read from by a deinterleaver/interleaver. Thus, TQ Delta's construction would consider portions of memory containing data previously stored by the interleaver/deinterleaver during a previous connection as being "used at the same time" as portions of memory actively being read from or written to by the deinterleaver/interleaver during a current connection. To illustrate the problem, suppose a transceiver's interleaver writes data to a specified memory location, the transceiver then reinitializes, the amount of memory required to interleave data bytes decreases, and as a result the specified memory location after re-

initialization falls in what Dr. Cooklev and TQ Delta characterize and illustrate (*see, e.g.*, Cooklev Dec. at ¶ 40; TQ Delta Brief at 14) as memory that is allocated to the interleaver, but not used. Under TQ Delta's proposed construction, that specified memory location, which falls outside the "used" area but within the "allocated" area, would be "used at the same time" as other portions of the memory being used by the deinterleaver because the specified memory location stores information at the same time that information is stored in, read from, or written to the shared memory allocated to the deinterleaver. The fact that the specified memory location stores stale information does not prevent the specified memory location from meeting TQ Delta's proposed construction. Thus, the inclusion of information that is merely stored in the shared memory in TQ Delta's proposed construction is contrary to the plain meaning of "used at the same time."

51. Furthermore, the prosecution history indicates that during an interview following a final rejection of the claims, "[t]he examiner and applicant discussed an overview of the invention and explained features of simultaneous transfer and types of interleaving and allocation of memory based on direction of transmission and bandwidth." A167 (D.I. 312, Ex. H) (emphasis added). For the interleaver and deinterleaver to simultaneously transfer information to and from the shared memory, the interleaver would need to be able to read from or write to the shared memory at the same time the deinterleaver was reading from or writing to the shared memory. In other words, the interleaver and deinterleaver would need active, simultaneous use of their allocated portions of the shared memory to enable simultaneous transfer of information.

52. Thus, in my opinion, a person having ordinary skill in the art at the time of the alleged invention would have understood "the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the

[interleaver/deinterleaver]" to mean "the deinterleaver/interleaver reads from or writes to its respective allocation of the shared memory at the same time as the interleaver/deinterleaver reads from or writes to its respective allocation of the shared memory" as Defendants propose.

E. "latency path"

53. In my opinion, a person having ordinary skill in the art at the time of the alleged invention would have understood "latency path" to mean "distinct transmit or receive path" as Defendants propose.

54. A person having ordinary skill in the art at the time of the alleged invention would have understood that transmit paths and receive paths have inherent latencies (delays). *See, e.g.*, A580 (G.992.1 (06/99)), § 5.1.1 (specifying both fast (non-interleaved) and interleaved paths and stating that "the 'fast' path provides low latency; the interleaved path provides very low error rate and greater latency"). The '890 patent explicitly defines latency as delay. A6 ('890 patent), 1:24-26 ("DSL systems carry applications that have different transmission requirements with regard to, for example, . . . latency (delay). . . ."). Because a skilled artisan at the time of the alleged invention would have known that every transmit path and every receive path causes some amount of delay, it would be circular to add the word "latency," and redundant to add the word "delay," to a construction of the term "latency path" that includes a "transmit or receive path."

55. Defendants' proposal that the transmit or receive path be "distinct" is supported by the intrinsic evidence, and it is consistent with how a person having ordinary skill in the art would have understood the claims, drawings, and written description. The claims in which this term appears identify distinct latency paths ("first" and "second" latency paths) for performing various interleaving/deinterleaving functions. *See* A61 ('473 patent), claim 19 ("a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency

path"); *id.*, claim 28 ("a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform an interleaving function associated with a first latency path, and perform a deinterleaving function associated with a second latency path"); A73 ('126 patent), claim 1 ("a multicarrier communications transceiver that is configured to perform a first interleaving function associated with a first latency path and perform a second interleaving function associated with a second latency path"), ('126 patent), claim 10 ("a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform a first deinterleaving function associated with a first latency path, and perform a second deinterleaving function associated with a second latency path"). The written description and drawings likewise describe and illustrate distinct latency paths. *See, e.g.*, A7 ('890 patent), 4:41-51 ("Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively."); FIG. 1 (illustrating distinct latency paths 210, 220, 310, 320). Thus, the claims, drawings, and written description all support Defendants' proposed construction.

F. "wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving/deinterleaving] function at any one particular time depending on the message"

56. In my opinion, a person having ordinary skill in the art at the time of the alleged invention would have understood "wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the message" to mean "wherein at least a number of bytes within the memory may be allocated to the [first] interleaving function or the [second interleaving /

deinterleaving] function at any one particular time depending on the amounts of memory specified in the message" as Defendants propose.

57. TQ Delta's proposed construction would have been unhelpful to a person having ordinary skill in the art at the time of the alleged invention because it is unclear what "at least some particular memory cells within the memory" means. As explained above in my discussion of the term "shared memory," it is unclear whether TQ Delta considers "memory" to be physical memory or addresses corresponding to, but divorced from, physical memory locations. Furthermore, and as also explained previously, TQ Delta's proposal to incorporate "memory cells" in the construed terms has no basis in the written description, drawings, or claims.

58. In contrast, Defendants' construction accurately characterizes how portions of memory are quantified—in bytes. This characterization is consistent with both the written description and the convention in the art of DSL at the time of the alleged invention, as explained above in my discussion of the term "amount of memory."

59. TQ Delta contends that "[n]othing in the specification supports Defendants' contention that an 'amount of memory' be specified in the message." TQ Delta Brief at 27. On the contrary, the written description states explicitly that the message received during initialization *always* specifies an amount of interleaver memory. *See, e.g.*, A7 ('890 patent), 4:24-28 ("a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths.");A9 ('890 patent), 8:9-21 (stating that message sent by first transceiver to second transceiver during initialization contains "Max Interleaver Memory" for latency paths #1, #2, and #3, and "Maximum total/shared memory for all latency paths," and that first transceiver

"select[s] latency path settings" based on this information); *id.*, 8:47-51 (same); *id.*, 8:62-67 ("a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver."). The written description emphasizes that in order for a "first modem" to determine framer/coder/interleaver (FCI) configuration parameters, which include the FEC parameters (N, R) and interleaver depth (D), "the first modem must know what are the capabilities of a second modem." *Id.*, 7:64-66 (emphasis added). Specifically, "the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space, the first modem must know the total shared memory for all transmitter latency paths." *Id.*, 8:1-5 (emphasis added). The information about memory constraints is provided in the message received during initialization. *See, e.g.*, *id.*, 8:9-51. Knowing the maximum amount of interleaver memory for each transmitter latency path and the total shared memory for all latency paths, "the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem." *Id.*, 8:5-8. As would have been understood by a person having ordinary skill in the art at the time of the alleged invention, the "configuration" referred to includes the allocation of shared memory among latency paths. Although the written description explains that "additional information can *also* be transmitted to the other transceiver and/or received from the other transceiver," (*id.*, 8:67-9:2), nowhere do the Family 3 patents disclose allocating memory based on a message, received during an initialization of a transceiver, that does *not* contain an indication of an amount of memory.

60. TQ Delta incorrectly suggests that Defendants' proposal somehow allows "the interleaver and deinterleaver to use the same physical locations (memory cells) of memory at the same time." TQ Delta Brief at 28. Defendants' proposed construction has nothing to do with requiring, and does not require, an interleaver to use the same physical locations at the same time. Defendants' proposal merely indicates that the interleaver and deinterleaver share memory— *i.e.*, the interleaver can read from/write to its memory allocation at the same time the deinterleaver can read from/write to its memory allocation.

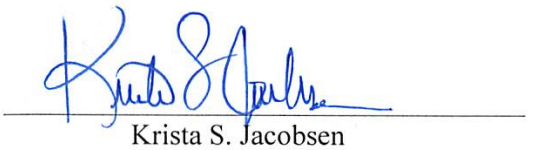
61. Furthermore, contrary to TQ Delta's assertion, Defendants' construction does not prohibit allocating the same quantity of bytes to each of the interleaver and the deinterleaver. Defendants' proposal merely indicates that a set of bytes ("a number of bytes") within the memory may be allocated to one of two functions at any one particular time. It does not preclude a different set of bytes that happens to be the same size from being allocated to the other of the two functions at the same time. Knowing that the term being construed is "wherein at least a portion of the memory may be allocated . . .," a person having ordinary skill in the art at the time of the alleged invention would have understood "a number of bytes within the memory" to refer to a set of bytes within the memory, and would not have concluded that however many bytes are in the "number of bytes within the memory" could not also be the quantity of bytes allocated to another function. A person having ordinary skill in the art would have recognized such an interpretation as absurd given the term being construed.

Thus, it is my opinion that a person having ordinary skill in the art at the time of the alleged invention would have understood "wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the message" to mean "wherein at least a number of

bytes within the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the amounts of memory specified in the message."

I declare under penalty of perjury of the laws of the United States that the foregoing is true and correct.

Date: July 19, 2017



Krista S. Jacobsen

Krista S. Jacobsen

1999 S. Bascom Ave., Suite 700, Campbell, CA 95008
E-mail: krista@jacobseniplaw.com; Tel: 408.455.5539 (M)

Experience

JACOBSEN IP LAW, Campbell, CA (February 2014 - present)
Attorney and Counselor at Law. Solo practitioner providing expert consultant, expert witness, patent litigation support, patent prosecution, and intellectual property (IP) counseling services.

SANTA CLARA UNIVERSITY SCHOOL OF LAW, Santa Clara, CA (January 2015 - present)
Lecturer in Law. Co-teaching Pretrial Litigation Techniques (Fall 2015, Fall 2016, Fall 2017) and Law Practice Management (Spring 2015, Spring 2016, Spring 2017).

DISRUPTIVE FORCE LLC, Campbell, CA (February 2015 - present)
Co-founder and CEO.

HEADWATER PARTNERS, Redwood Shores, CA (July 2011 - February 2014)
Head Counsel. Responsibilities included general counsel duties and patent prosecution.

COVINGTON & BURLING, LLP, Redwood Shores, CA (October 2009 - July 2011)
Associate. IP litigation.

HELLER EHRMAN, Menlo Park, CA (May-July 2008)
Summer Associate. IP litigation. Researched and drafted legal memoranda and briefs.

BLAKELY SOKOLOFF TAYLOR & ZAFMAN, Sunnyvale, CA (June-August 2007)
Summer Associate. Patent prosecution. Composed responses to United States Patent and Trademark Office office actions and wrote portions of patent applications, including claims.

CONSULTANT (July 2004 - September 2007)
Responsibilities included assisting clients to determine and execute digital subscriber line (DSL) standardization and product strategies, writing simulations, generating and presenting technical tutorials, drafting and prosecuting patent applications, and helping with other patent issues. Clients included 2Wire, Inc., PMC-Sierra, Atheros Communications, and Beyer Law Group.

TEXAS INSTRUMENTS (TI) (formerly AMATI COMMUNICATIONS), San Jose, CA (January 1994 - May 2004).

Lead xDSL Standards Strategist (2001-04)

- Led TI's DSL standardization efforts, managed standards resources and budget, and communicated standards progress and status within TI.
- Developed and presented dozens of technical proposals for regional and international standards organizations, including ETSI TM6, ITU-T SG15/Q4, T1E1.4, and IEEE 802.3ah (Ethernet in the first mile).
- Wrote DSL white papers, technical reports, technical book chapters, and articles for external publications.
- Participated as a member of business unit patent committee and worked with TI legal department to ensure protection of intellectual property and to provide technical assistance.
- Wrote and ran DSL system simulations.
- Made presentations at industry conferences and events.

Previous roles with Amati/TI were *Project Manager, ADSL over ISDN* (2000-01), *Project Manager, VDSL* (1999-2000), *Senior Staff Engineer* (1998-99), *Staff Engineer* (1997-98), *Senior Systems Engineer* (1996-97), *Consultant* (1994-96).

VITEL COMMUNICATIONS CORPORATION, Santa Clara, CA (August 1991 - May 1992).
Member of telecommunications group. Worked on a team that developed a video telephony transceiver.

Bar Memberships and Registrations

STATE BAR OF CALIFORNIA
Member No. 267868 (admitted December 7, 2009)

COLORADO STATE BAR
Registration No. 43,294 (admitted May 24, 2011 (currently inactive))

UNITED STATES PATENT AND TRADEMARK OFFICE
Registration No. 59,374 (registered October 11, 2006)

Krista S. Jacobsen

Education

SANTA CLARA UNIVERSITY SCHOOL OF LAW (Santa Clara, CA)

JD (*magna cum laude*), 2009

Honors and Awards

- Santa Clara University School of Law Intellectual Property (IP) Fellowship (2006-09)
- Dean's List (2006-09)
- Order of the Coif (2009)
- ABA-BNA Award for Excellence In the Study of Intellectual Property Law (Spring 2008)
- CALI Award for Execllence In: Managing Complex IP Litigation (Fall 2008), IP Litigation Techniques (Spring 2008), Patent Prosecution (Spring 2008), Protection of IP (Spring 2008), Advocacy (Fall 2007), Contracts (Spring 2007)
- Witkin Award for Excellence In: Opening Statements and Closing Arguments (Fall 2008), Pretrial Litigation Techniques (Fall 2008), Mass Communication (Fall 2007), Property (Spring 2007), Legal Analysis, Research and Writing, Section H (Spring 2007)
- Grand Prize, First Annual San Francisco Intellectual Property Law Association Student Writing Competition (February 2009)
- Selected to represent Santa Clara University in the Dean Jerome Prince Memorial Evidence Moot Court Competition (Spring 2009) and Constance Baker Motley National Moot Court Competition in Constitutional Law (Spring 2008)

Activities

- Co-President, Santa Clara University Student Intellectual Property Law Association (2008-09)
- Vice President, Alumni Relations, Santa Clara University Intellectual Property Association (2007-08)
- Associate, Santa Clara Computer and High Tech Law Journal (2007-08)

STANFORD UNIVERSITY (Stanford, CA)

Ph.D. in electrical engineering, 1996

- Dissertation: *Discrete Multi-Tone-Based Communications in the Reverse Channel of Hybrid Fiber-Coax Networks*
- Adviser: John M. Cioffi (http://www.stanford.edu/group/cioffi)

MSEE, 1993

- Digital communications specialization

Honors and Awards

- IBM Graduate Fellowship (1994-95)
- National Science Foundation Graduate Fellowship (1991-94)
- IEEE Communications Society Scholarship (1993)

UNIVERSITY OF DENVER (Denver, CO)

BSEE (*summa cum laude*), 1991

- Communications specialization

Honors and Awards

- Winner, Denver Section IEEE Student Paper Contest (1991)
- University of Denver Pioneer Award (1991)
- University of Denver Distinguished Senior Woman Award (1990)
- Phi Beta Kappa (1988)
- University of Denver Honors Scholarship (1986-91)
- Colorado Scholars Scholarship (1987-91)

Publications

LAW REVIEW AND JOURNAL PAPERS

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Krista S. Jacobsen

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Author of the chapter entitled "Last Mile Copper Access" in *Broadband Last Mile Access Technologies for Multimedia Communications* (Nikil Jayant, ed., CRC Press, 2005).

Author of the definition of "broadband communication" in *World Book Encyclopedia* (2003).

TECHNICAL JOURNAL PAPERS AND MAGAZINE ARTICLES

K.S. Jacobsen. "Patents and Standardization, Part 3: Commitments to License Standard-Essential Patents Under Reasonable and Non-Discriminatory (RAND) Terms." *IEEE Communications Magazine - Communications Standards Supplement*, September 2016, pp. 66-71.

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J.M. Cioffi *et al*. "Very-high-speed Digital Subscriber Lines." In *IEEE Communications Magazine*, vol. 37, no. 4, April 1999, pp. 72-79.

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K.S. Jacobsen. "Design and Performance of Synchronized DMT (SDMT) Modems for VDSL." In *ICCE Conference Record*, Los Angeles, CA, June 1999.

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K.S. Jacobsen. "Discrete Multi-Tone Modulation for High-Speed Upstream Communications on HFC Networks." In *Conference Record of the Thirty-First Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 1997.

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J.A.C. Bingham and K.S. Jacobsen. "Upstream Transmission in an HFC System using SDMT: the Network, Data Rates, and a MAC Protocol." Presented at Globecom '95, Singapore, November 1995.

Krista S. Jacobsen

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K.S. Jacobsen and J.M. Cioffi. "High-performance Multimedia Transmission on the Cable Television Network." In *Proceedings 1994 International Conference on Communications*, New Orleans, LA, May 1994.

Patents

A.J. Redfern, G. Ginis, F.A. Mujica, and K.S. Jacobsen. "Spectrally flexible band plans with reduced filtering requirements." U.S. Patent Number 7,342,937. March 2008.

K.S. Jacobsen, M.D. Agah, and B.R. Wiese. "Method to mitigate effects of ISDN off/on transitions in ADSL." U.S. patent number 7,184,467. February 2007.

J.M. Cioffi, J.A.C. Bingham, and K.S. Jacobsen. "Method and apparatus for coordinating multi-point to-point communications in a multi-tone data transmission system." U.S. patent number 7,110,370. September 2006.

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J.M. Cioffi, J.A.C. Bingham, and K.S. Jacobsen. "Method and apparatus for coordinating multi-point to-point communications in a multi-tone data transmission system." U.S. patent number 6,937,623. August 2005.

K.S. Jacobsen, B. Wiese, and C. Milbrandt. "Upstream power back-off." U.S. patent number 6,922,448. July 2005.

J.M. Cioffi, J.A.C. Bingham, and K.S. Jacobsen. "Method and apparatus for coordinating multi-point to-point communications in a multi-tone data transmission system." U.S. patent number 6,473,438. October 2002.

B. Wiese, K.S. Jacobsen, N.P. Sands, and J. Chow. "Initializing communications in systems using multi-carrier modulation." U.S. patent number 6,434,119. August 2002.

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J.A.C. Bingham and K.S. Jacobsen. "Methods for coordinating upstream discrete multi-tone data transmissions." U.S. patent number 5,644,573. July 1997.

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC. Defendant.	Civil Action No. 13-cv-1835-RGA
TQ DELTA, LLC, Plaintiff, v. ZHONE TECHNOLOGIES, INC. Defendant.	Civil Action No. 13-cv-1836-RGA
TQ DELTA, LLC, Plaintiff, v. ZYXEL COMMUNICATIONS, INC. and ZYXEL COMMUNICATIONS CORPORATION, Defendants.	Civil Action No. 13-cv-2013-RGA
TQ DELTA, LLC, Plaintiff, v. ADTRAN, INC. Defendant.	Civil Action No. 14-cv-954-RGA
ADTRAN, INC, Plaintiff, v. TQ DELTA, LLC. Defendant.	Civil Action No. 15-cv-121-RGA

RESPONSE DECLARATION OF DR. TODOR COOKLEV IN SUPPORT OF TQ DELTA'S FAMILY 3 CLAIM CONSTRUCTION BRIEF

I. Introduction

1. I incorporate my declaration in support of Plaintiff's opening claim construction brief, served on June 21, 2017 ("my Opening Declaration"), into this declaration.

2. In addition to the information disclosed in my Opening Declaration, I have also relied on Defendants' answering claim construction brief and Dr. Krista Jacobsen's declaration in support of Defendants' answering claim construction brief, served on July 19, 2017 ("Dr. Jacobsen's Answer Declaration" or "the Jacobsen Decl.").

3. I have prepared this Declaration to address issues in the Jacobsen Decl. that are relevant to the parties' respective claim construction positions.

4. My failure to expressly reference or correct any portion of the Jacobsen Decl. is not an admission that I agree with the accuracy of those portions. This declaration does not constitute a waiver of any other arguments I may have with respect to opinions in the Jacobsen Decl. I retain my right to address or opine on at a later date any opinions in the Jacobsen Decl.

5. In particular, this declaration addresses the following claim terms:

Term	Claims
"transceiver"	'890 patent, claim 5, '381 patent, claim 5 '882 patent, claim 13, '048 patent, claim 1, '473 patent, claim 19, 28, and '126 patent, claims 1, 10
"shared memory"	'890 patent, claim 5, '381 patent, claim 5, '882 patent, claim 13, and '048 patent, claim 1
"wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving/deinterleaving] function at any one particular time depending on the message"	'473 patent, claim 19 and '126 patent, claim 1

"the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]"	'890 patent, claim 5, '381 patent, claim 5, '882 patent, claim 13, and '048 patent, claim 1

II. Background of the Technology

6. Dr. Jacobsen asserts that "[F]urthermore, a person having ordinary skill in the art at the time of the alleged invention would not have referred to "memory cells" in the context of the Family 3 patents, which present the alleged invention as applied to DSL." *See* Jacobsen Declaration at ¶ 24. I disagree. As an initial matter, a POSITA would understand that a memory cell is a physical unit of solid state memory. Each memory cell will typically story one bit of data. A memory cell can be built using different electronic technologies such as bipolar and MOS transistors. Memory cells are taught by almost every textbook on computer architecture, including *Computer Architecture: From Microprocessors to Supercomputers*, by B. Parhami, Oxford University Press, published in 2004.

7. Based on implementation and the architecture of the memory, the smallest addressable unit of memory may be a byte, i.e., 8 bits of data or 8 memory cells. In other words, data is stored, read, and written at least 8 bits at a time. But this does not change the fact that memory is made up of physical memory cells. In the context of the claims of the Family 3 Patents, a POSITA would recognize that the shared memory used by the interleaver and deinterleaver is comprised of physical memory cells or units of memory.

8. The Jacobsen Declaration at ¶ 60, for example, agrees that the portions of the shared memory allocated and used by the interleaver and deinterleaver are specific physical memory locations. At ¶ 61, the Jacobsen Declaration confirms that sets of bytes within the memory may be allocated to either the interleaver or the deinterleaver. Thus, there is no dispute that shared

memory is comprised of physical memory locations and the interleaver/deinterleaver uses its respective allocation of physical memory locations of the shared memory to read, write and store information.

III. Disputed Claim Terms

A. "transceiver"

9. Dr. Jacobsen asserts that "[t]he common circuit requirement would introduce confusion into the term, because a person having ordinary skill in the art at the time of the alleged invention would not know how much circuitry would have to be "common" to meet the claim". *See* Jacobsen Declaration at ¶ 27. I disagree because the claim does not require this determination. Consequently it is not necessary to determine how much circuitry has to be common to find infringement.

10. The '890 patent explicitly requires the transmitter portion and the receiver portion of the transceiver to share circuitry:

> A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory.

A1 ('890 patent) at Abstract.

> Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120.

A8 ('890 patent) at 5:40-42.

> Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

A6 ('890 patent) at 2:40-44.

> The transceiver 100 further includes a shared processing module 110, a shared

> memory 120, a parameter determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

A7 ('890 patent) at 4:51-56.

> Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

A8 ('890 patent) at 5:53-56.

11. Consequently, in the context of the Family 3 patents, a person of skill would understand that sharing circuitry between the transmitter and receiver, when each is a part of a single transceiver, to be an inherent characteristic of that transceiver.

12. Dr. Jacobsen also tries to make a distinction between wireless transceivers and DSL transceivers and asserts that "[b]ecause the design constraints (*e.g.*, power, size, etc.) for wireless transceivers differ from those for DSL transceivers, the definitions Dr. Cooklev cites would not have been considered controlling by a person having ordinary skill in the art of DSL." *See* Jacobsen Declaration at ¶ 30. I disagree at least because the design constraints of power and size are irrelevant to the definition of a transceiver. The '890 patent also specifies that it can be implemented on wired and/or wireless devices: "the exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment" (A7 ('890 patent) at 3:6-8), and also "[t]he above-described system can be implemented on wired and/or wireless telecommunications devices" (A10 ('890 patent) at 9:38-39). Therefore, Dr. Jacobsen's statement is unsupported.

B. "shared memory"

13. Dr. Jacobsen contends that "[t]he written description repeatedly refers to the shared memory as a singular object." *See* Jacobsen Declaration at ¶ 35. The rationale for Dr. Jacobsen's opinion is that "[e]ach of the asserted claims in which this term appears refers only to

"a" or "the" shared memory, which implies that there is only one single memory." *See* Jacobsen Declaration at ¶ 36.

14. The use of "a" or "the" does not establish that the shared memory is a single object. When using "a" or "the" the Family 3 patents refer to the shared property of the memory, but do not discuss implementations of this shared memory. The Family 3 patents can be implemented using "an ASIC or other integrated circuit." A10 ('890 patent) at 9:53-54. I agree with Dr. Jacobsen that on some integrated circuits the shared memory may be a single object. However, I disagree that it must necessarily be a single object. On some integrated circuits the shared memory may be implemented using multiple blocks of memory. Consequently, it would be technically incorrect to restrict the meaning of the claim term to only a *single* common memory.

15. Dr. Jacobsen also contends that "TQ Delta's proposal introduces confusion in the construction of the term 'shared memory' because it is unclear whether a 'common memory space' refers to software or hardware." *See* Jacobsen Declaration at ¶ 38. The term "common memory space" is not confusing at least because a POSITA would understand common memory space to mean the physical memory. The Family 3 Patent specifically refers to this physical shared memory as a common memory space. A9 ('890 Patent) at 8:3-4. Accordingly, a POSITA in light of the specification would understand that shared memory in relevant part is a "common memory space."

16. Dr. Jacobsen also states that "[a] person having ordinary skill in the art at the time of the alleged invention could well have considered a group of memory modules to be "multiple separate and discrete blocks of memory," and therefore it is unclear what physical element or elements Dr. Cooklev believes constitute 'shared memory.'" To clarify, a POSITA would recognize that "multiple separate and discrete blocks of memory" may nevertheless be organized

so that they together constitute a single memory space. A POSITA would realize such an arrangement using a common memory addressing scheme, for example.

17. Dr. Jacobsen also asserts that "there is nothing in the Family 3 patents that supports TQ Delta's reading of "memory cells" into the claims, particularly when the term "memory cells" is not used anywhere in the patents." *See* Jacobsen Declaration at ¶ 40. I disagree at least because, as explained above, a memory cell is the smallest unit of physical memory. A memory cell can be built using different electronic technologies such as bipolar and MOS transistors. The term "memory cell" is well-known to a POSITA.

18. Dr. Jacobsen, at ¶ 38 of her declaration, also cites to a dictionary definition (found at A556) for shared memory. This definition provides that shared memory is the "use of the same portion of memory by two distinct processes, or memory so shared." This definition is consistent with my understanding of shared memory to the extent that a particular portion of shared memory can be used by one or the other of two processes (e.g., interleaver or deinterleaver) at different times depending on the process to which that portion is allocated. However, in view of Dr. Jacobsen's understanding the Family 3 Patents, the definition is incomplete and ambiguous. Specifically, at ¶ 61 Dr. Jacobsen notes that sharing memory in the context of the Family 3 Patents means that "the interleaver can read from/write to its memory allocation [of the memory] at the same time the deinterleaver can read from/write to its memory allocation [of the memory]." The dictionary definition does not account for the exclusive use (read/write/store) by the interleaver or deinterleaver of the portion of common memory that has been allocated to the interleaver or deinterleaver. Although, the interleaver and deinterleaver can use their respective allocations of common memory concurrently, at any given time, only the portion of shared memory that was allocated to the interleaver may be used by the interleaver

and only the portion of shared memory that was allocated to the deinterleaver may be used by the deinterleaver. . The dictionary definition cited by Dr. Jacobsen does not clarify this concurrent yet exclusive use by the interleaver and deinterleaver of their respective memory allocations.

19. The second part of the definition cited by Dr. Jacobsen, which refers to the use of shared memory for interprocess communication, conflicts with the Family 3 Patents usage of shared memory and Dr. Jacobsen's understanding of shared memory at ¶¶ 60 and 61. As explained in the prior paragraph, the interleaver and deinterleaver use (read from/write to/store within) their respective allocations of common memory concurrently. Further, the interleaver and deinterleaver exclusively use their respective allocations of common memory. Therefore, the interleaver and deinterleaver do not use the shared memory to communicate with each other. Although, use of memory for interprocess communication is another type of memory sharing, it is not the type of memory sharing contemplated by the Family 3 Patents. When used for interprocess communication, typically one process writes to the memory information that the other process will read from the memory. In this way, interprocess communication is facilitated.

C. "wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving/deinterleaving] function at any one particular time depending on the message"

20. Dr. Jacobsen notes that, in the context of the Family 3 Patents, the interleaver and deinterleaver do not use the same physical locations of the shared memory at the same time. *See* Jacobsen Decl. at ¶ 60. I agree with this.

21. Further, at ¶ 61 of her declaration, Dr. Jacobsen asserts that, under the Defendants' construction, a set of bytes within the shared memory may be allocated for use by only one of the two functions (interleaver or deinterleaver) at any one particular time.

22. Based on my understanding of ¶¶ 60 and 61 of the Jacobsen Declaration, it appears both TQ Delta and Defendants agree that "portion of memory," in relevant part means, particular

physical locations of the shared memory. However, Defendants' construction is ambiguous because "number of bytes" could be interpreted to simply mean a numeric value of bytes. Defendants' construction does not account for Defendants' understanding that portion of memory means particular physical locations of the shared memory.

D. "the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]"

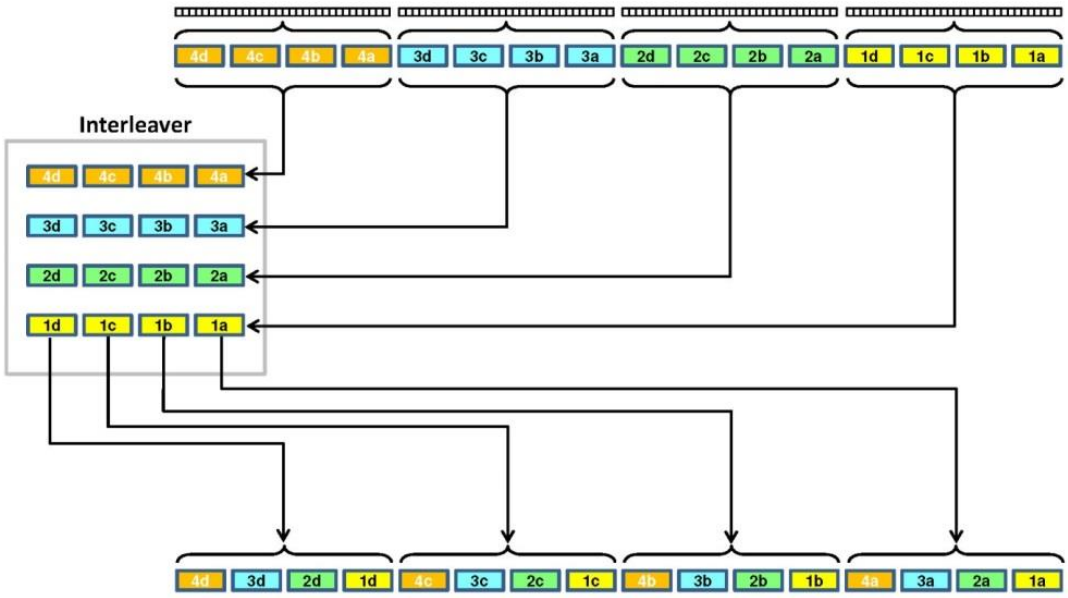
23. Dr. Jacobsen cites an interview record from the prosecution history of one of the Family 3 patents, which states "[t]he examiner and applicant discussed an overview of the invention and explained features of simultaneous transfer and types of interleaving and allocation of memory based on direction of transmission and bandwidth." Jacobsen Declaration at ¶ 51 (quoting A167 (12/16/2009 Interview Summary) (summarizing 12/8/2009 interview)). Based on this statement from the interview summary, Dr. Jacobsen concludes that "[f]or the interleaver and deinterleaver to simultaneously transfer information to and from the shared memory, the interleaver would need to be able to read from or write to the shared memory at the same time the deinterleaver was reading from or writing to the shared memory." *Id.* I disagree with Dr. Jacobsen's conclusion for several reasons.

24. First, Dr. Jacobsen incorrectly interprets the reference by the examiner to "simultaneous transfer" as referring to transfer to and from the shared memory. There is no basis for concluding that the referenced "transfer" is to and from memory. The examiner's summary does not state that the transfer is to/from memory and the Family 3 patent specification does not use the term transfer in describing use of the memory. Instead, I understand the examiner's reference to "simultaneous transfer" to be referring to the fact that transmission and reception of data are occurring simultaneously and, therefore, the shared memory is being used concurrently by the interleaver and deinterleaver. My interpretation of the examiner's statement is supported

by the fact that the Office Action that the examiner issued on the day after the examiner interview identifies as a primary topic "how the same memory can be *used for simultaneously receiving of data and transmitting data*" and states "it is noted that the features upon which applicant relies (i.e., the same memory being *used for simultaneously receiving of data and transmitting data*) are not recited in the claims. A148 (12/9/2009 Office Action at p. 2). There is no discussion in the Office Action of simultaneous transfer to/from memory.

25. Dr. Jacobsen is incorrect to the extent her opinion is that the simultaneous transmission and reception of data necessarily requires that "the interleaver would need to be able to read from or write to the shared memory at the same time the deinterleaver was reading from or writing to the shared memory. Rather, all that is required is that the shared memory can be used simultaneously by the interleaver and deinterleaver. And as I previously stated, memory is being "used" by an interleaver or deinterleaver function when the memory is passively storing, in addition to actively reading or writing, data relating to the function.

26. The use of memory for the passive act of storing (i.e., temporarily holding) data while it is being interleaved is an integral part of the function of interleaving as was explained in my prior declaration at ¶¶ 16-32. Dr. Jacobsen agreed with this explanation. *See* Jacobsen Decl. at ¶ 16. My illustration of a simple interleaver that I previously set forth in my Opening Declaration is reproduced below.



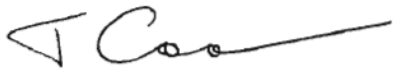
27. As I explained in my prior declaration, "the first groups of bits from the four different codewords (yellow #1a, green #2a, blue #3a, and orange #4a) is transmitted first; then a second group of bits from each codeword (yellow #1b, green #2b, blue #3b, and orange #4b) are transmitted and so on." A_ (Cooklev Decl.) at ¶ 25. In DSL the block of codewords is transmitted serially transmitted as a serial stream of DMT symbols. Thus, a non-infinitesimally small amount of time elapses before the transmission of the four groups of bits is complete. During this time, the groups of bits are stored in the interleaver memory. This storage is necessary so that the order of the groups of bits can be rearranged (i.e., interleaved). Thus, a POSITA would understand that, with regards to the interleaver, use of memory in the context of the claims would include reading, writing and storing of information.

28. With respect to the deinterleaver at the receiver, as I previously stated "the first group of yellow bits (yellow #1a) must be stored while waiting for the second group (yellow #1b), third (yellow #1c), and fourth group (yellow #1d) of yellow bits to be received. Only after receipt of all of the bits of a codeword can the codeword be decoded." A_ (Cooklev Decl.) at

¶ 27. While the deinterleaver is waiting for all groups of bits for a given codeword to be received, the already received group of bits is stored in deinterleaver memory. This is necessary so that the groups of bits may be arranged back into their original order. Thus, a POSITA would understand that, with regards to the deinterleaver, use of memory in the context of the claims would include reading, writing and storing of information.

29. Dr. Jacobsen constructs a hypothetical example to illustrate that under TQ Delta's construction a memory location that "stores stale information would" nevertheless meet TQ Delta construction. *See* Jacobsen Declaration at ¶ 50. This mischaracterizes what it means to use memory by storing information. Memory is used for storage by an interleaver or deinterleaver when the memory stores information waiting to be transmitted, or stores received information that has not been processed. Once the information is transmitted or processed, the information is no longer relevant and the interleaver/deinterleaver can use the same memory to store the next block of information to be interleaved or deinterleaved. A POSITA would recognize that once the information in the memory is transmitted or processed, it is no longer being "used" by the interleaver or deinterleaver. Stale information is not used and, consequently, the memory that is storing the stale information is no longer being used by the interleaver or deinterleaver.

I declare under penalty of perjury that the foregoing is true and correct.



Dated: August 9, 2017

Dr. Todor Cooklev

UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC., Defendant.	Civil Action No. 13-cv-1835-RGA
TQ DELTA, LLC, Plaintiff, v. ZHONE TECHNOLOGIES, INC., Defendant.	Civil Action No. 13-cv-1836-RGA
TQ DELTA, LLC, Plaintiff, v. ZYXEL COMMUNICATIONS, INC., and ZYXEL COMMUNICATIONS CORPORATION, Defendants.	Civil Action No. 13-cv-2013-RGA
TQ DELTA, LLC, Plaintiff, v. ADTRAN, INC., Defendant.	Civil Action No. 14-cv-954-RGA
ADTRAN, INC., Plaintiff, v. TQ DELTA, LLC, Defendant.	Civil Action No. 15-cv-121-RGA

DECLARATION OF DR. KRISTA S. JACOBSEN IN SUPPORT OF DEFENDANTS' FAMILY 3 CLAIM CONSTRUCTION BRIEF

I. INTRODUCTION

1. I am providing this declaration in support of Defendants' Sur-Reply Claim Construction Brief For the Family 2 Patents.

2. In addition to the materials I reviewed to prepare my declaration in support of Defendants' claim construction brief ("my previous declaration"), which included "Plaintiff's Opening Claim Construction Brief For Family 3" ("TQ Delta Opening Brief") and the "Declaration of Dr. Todor Cooklev In Support of TQ Delta's Family 3 Claim Construction Brief" ("Cooklev First Dec."), in preparing this declaration I have also reviewed "Plaintiff's Reply Claim Construction Brief For Family 3 Patents" ("TQ Delta Reply Brief") and the "Response Declaration of Dr. Todor Cooklev In Support of TQ Delta's Family 3 Claim Construction Brief" ("Cooklev Reply Dec.").

II. DISPUTED CLAIM TERMS

A. "shared memory"

3. Dr. Cooklev asserts that "a POSITA would understand common memory space to mean the physical memory." Cooklev Reply Dec. at ¶ 15. Citing column 8, lines 3-4 of the '890 patent, he states that "[t]he Family 3 Patent specifically refers to this physical shared memory as common memory space." *Id.* But the cited portion of the Family 3 patents does not refer to physical shared memory as "common memory space," or otherwise define what a "common memory space" is. All it says is that "since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths." '890 patent at col. 8:3-4. There is no indication, here or elsewhere, what the term "common memory space" means, much less that it means "physical shared memory." In fact, the Family 3 patents do not use the term "common memory space" anywhere else, and, as I stated in my previous declaration, a person having ordinary skill in the art at the time of the

alleged invention would not have known whether "common memory space" means the physical storage locations of a memory—*i.e.*, hardware—or a collection of software addresses, corresponding to and identifying physical storage locations, that are divorced from the physical memory implementation.

4. TQ Delta points to the only use of the term "common memory space" in the Family 3 patents' specification as allegedly supporting its proposed construction. TQ Delta Reply Brief at 5. But the issue is not whether the Family 3 patents use the term "common memory space;" rather, the issue is that the term "common memory space" would have been unclear to a person having ordinary skill in the art at the time of the alleged invention. TQ Delta characterized its own proposal as an "attempt to clarify that common memory space refers to hardware (particular memory cells)." TQ Delta Reply Brief at 6. In my opinion, this supposed clarification does little good, and the ambiguous term "common memory space" is not necessary and should not be included in the construction. A person having ordinary skill in the art at the time of the alleged invention would have understood the specification to refer to the "shared memory" as "a single common memory."

B. "the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]"

5. In response to my observation that TQ Delta's proposed construction would characterize portions of the shared memory previously written by an interleaver/deinterleaver as being "used at the same time" as memory actively being written to or read from by a deinterleaver/interleaver, Dr. Cooklev and TQ Delta now introduce the notion of a constantly-changing, time-varying amount of "used" shared memory that depends on whether a particular memory location has been read recently enough by the interleaver or deinterleaver. Specifically, Dr. Cooklev and TQ Delta contend that "[o]nce the information is transmitted or processed, the

information is no longer relevant and the interleaver/deinterleaver can use the same memory to store the next block of information to be interleaved or deinterleaved." Cooklev Reply Dec. at ¶ 29; TQ Delta Reply Brief at 12. Dr. Cooklev opines that "once the information in the memory is transmitted or processed, it is no longer being 'used' by the interleaver or deinterleaver. Stale information is not used and, consequently, the memory that is storing the stale information is no longer being used by the interleaver or deinterleaver." Cooklev Reply Dec. at ¶ 29.

6. Dr. Cooklev thus recognizes that when information stored in memory is read, that information does not disappear from the memory by virtue of having been read. It remains stored in the memory until overwritten. Thus, according to Dr. Cooklev and TQ Delta, "used" shared memory includes only those memory locations (a) that are actively being read from or written to by the interleaver or deinterleaver (Defendants' proposal), and (b) that have been written to, but not yet read from, by the interleaver or deinterleaver.

7. But, as a person having ordinary skill in the art at the time of the alleged invention would have recognized, TQ Delta's proposed construction does not capture this newly-introduced distinction in what it means for information to be "stored" in shared memory. A skilled artisan would not have understood TQ Delta's proposed construction of "information is stored in, read from, or written to the shared memory allocated to the deinterleaver at the same time that information is stored in, read from, or written to the shared memory allocated to the interleaver" to exclude information that has been stored in the memory but that Dr. Cooklev contends is no longer "used" because it has been read.

8. TQ Delta and Dr. Cooklev also criticize my interpretation of the examiner interview summary from the '890 patent's prosecution history, (TQ Delta Reply Brief at 10-11; Cooklev Reply Dec. at ¶¶ 23-24), but the applicant's amendments to the claims after the

examiner interview confirm that my interpretation—namely, that the "simultaneous transfer" refers to transfers to and from memory—is the correct one.

9. At the time of the interview, claims 1-45 were pending. A147 (Office Action, 12/9/2009), at 1. The subject of the examiner interview was claim 1 (*see* A653 (Interview Summary, 12/16/2009), which recited, in its entirety:

> A method for sharing resources in a transceiver comprising:
> allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

A658 (Amdmt. & Resp., 8/21/2009).

10. TQ Delta and Dr. Cooklev contend that "the examiner's reference to 'simultaneous transfer' is referring to the fact that transmission and reception of data are occurring simultaneously and, therefore, the shared memory is being used concurrently by the interleaver and deinterleaver." TQ Delta Reply Brief at 11; *see also* Cooklev Reply Dec. at ¶ 24. In support, Dr. Cooklev and TQ Delta cite the Final Rejection sent the day after the examiner interview, in which the examiner responded to the applicant's argument that the prior art did not anticipate claim 1 by stating that "it is noted that the features upon which applicant relies (i.e., the same memory being used for simultaneously receiving of data and transmitting data) are not recited in the rejected claim(s)." TQ Delta Reply Brief at 11; Cooklev Reply Dec. at ¶ 24; *see also* A148 (Office Action, 12/9/09). In arguing the alleged patentability of claim 1 over the cited reference, the applicant had stated, "Fadavi-Ardekani is not enabling for how the same memory can be used for simultaneous receiving of data and transmitting of data." A663 (Amdmt. & Resp, 8/21/2009) at 8.

11. In response to the Final Rejection, the applicant canceled claims 1-45 and added a new independent claim 46, which recited:

> A method of allocating shared memory in a transceiver comprising:
> transmitting or receiving, by the transceiver, a message during initialization indicating a maximum number of bytes of memory that can be allocated to an interleaver;
> allocating, in the transceiver, a first number of bytes of a shared memory to an interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate; and
> allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality RS coded data bytes received at a second data rate,
> wherein the allocated memory for the interleaver does not exceed the maximum number of bytes indicated in the message, and
> wherein the shared memory is used to simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes.

A648-649 (Amdmt. & Resp., 12/17/2009), at 2.

Based on the similarities between claim 46 and the asserted claims, and the fact that neither says anything about "simultaneously receiving of data and transmitting data," the implication is that the discussed "simultaneous transfer" did indeed refer to the use of the shared memory to "simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes." As a person having ordinary skill in the art at the time of the alleged invention would have understood, being able to "simultaneously interleave . . . and deinterleave" would require the interleaver to be able to read from or write to the shared memory at the same time the deinterleaver is reading from or writing to the shared memory.

C. "wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving/deinterleaving] function at any one particular time depending on the message"

12. TQ Delta argues that "[n]othing in the claims or the specification requires that that amounts of memory be specified in the message." TQ Delta Reply Brief at 17. TQ Delta also contends that "[a] transceiver may know sufficient information to allocate portions of memory without the message specifying 'amounts of memory.'" TQ Delta Reply Brief at 18.

On the contrary, and as I explained in my previous declaration, the written description does not provide a single embodiment in which the message *does not* specify an amount of memory. Instead, it states explicitly that the message received during initialization *always* specifies *at least* some amount of interleaver memory. *See, e.g.*, '890 patent at col. 4:24-28 ("a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths.") (emphasis added); *id.* at col. 8:9-21 (stating that message sent by first transceiver to second transceiver during initialization contains "Max Interleaver Memory" for latency paths #1, #2, and #3, and "Maximum total/shared memory for all latency paths," and that first transceiver "select[s] latency path settings" based on this information); *id.* at col. 8:47-51 (same); *id.* at col. 8:62-67 ("a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver.") (emphasis added).

13. Although the written description explains that "additional information can *also* be transmitted to the other transceiver and/or received from the other transceiver," (*id.* at col. 8:67-9:2 (emphasis added)), nowhere do the Family 3 patents disclose allocating memory based on a message, received during an initialization of a transceiver, that does not *at least* contain an indication of an amount of memory. Thus, in my opinion, one of ordinary skill in the art would understand that the "message" in this term would specify an amount of memory.

I declare under penalty of perjury of the laws of the United States that the foregoing is true and correct.

Date: August 23, 2017

Krista S. Jacobsen